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JUNE 8
Issue 12/2006
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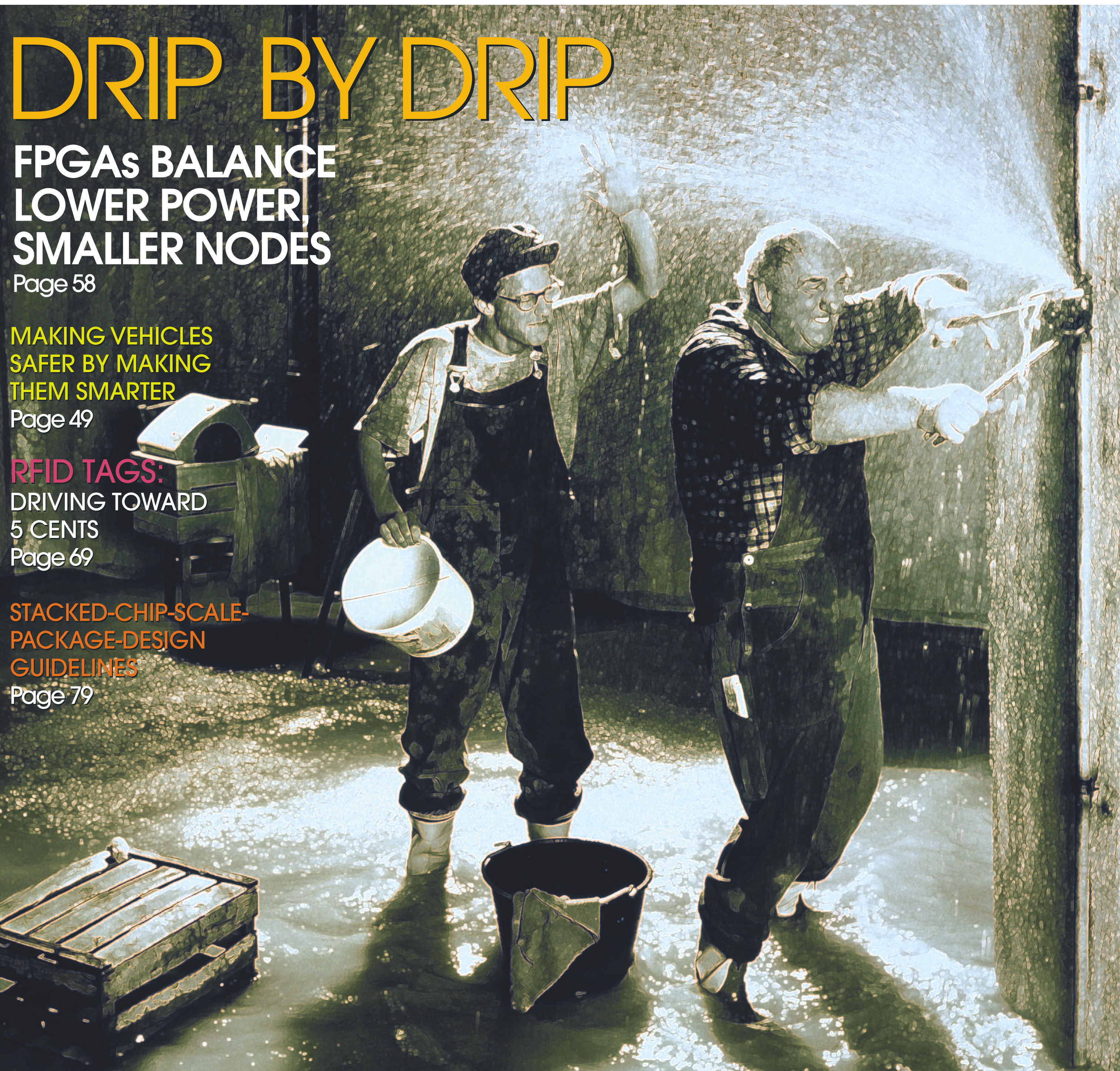
Will a **Reality Check** poke a hole in broadband from airships? Pg 110

Bonnie Baker chooses antialiasing-filter amplifiers Pg 44

Our **Prying Eyes** break down a broken cell phone Pg 46

Design Ideas Pg 87



DRIP BY DRIP

FPGAs BALANCE LOWER POWER, SMALLER NODES

Page 58

MAKING VEHICLES SAFER BY MAKING THEM SMARTER

Page 49

RFID TAGS: DRIVING TOWARD 5 CENTS

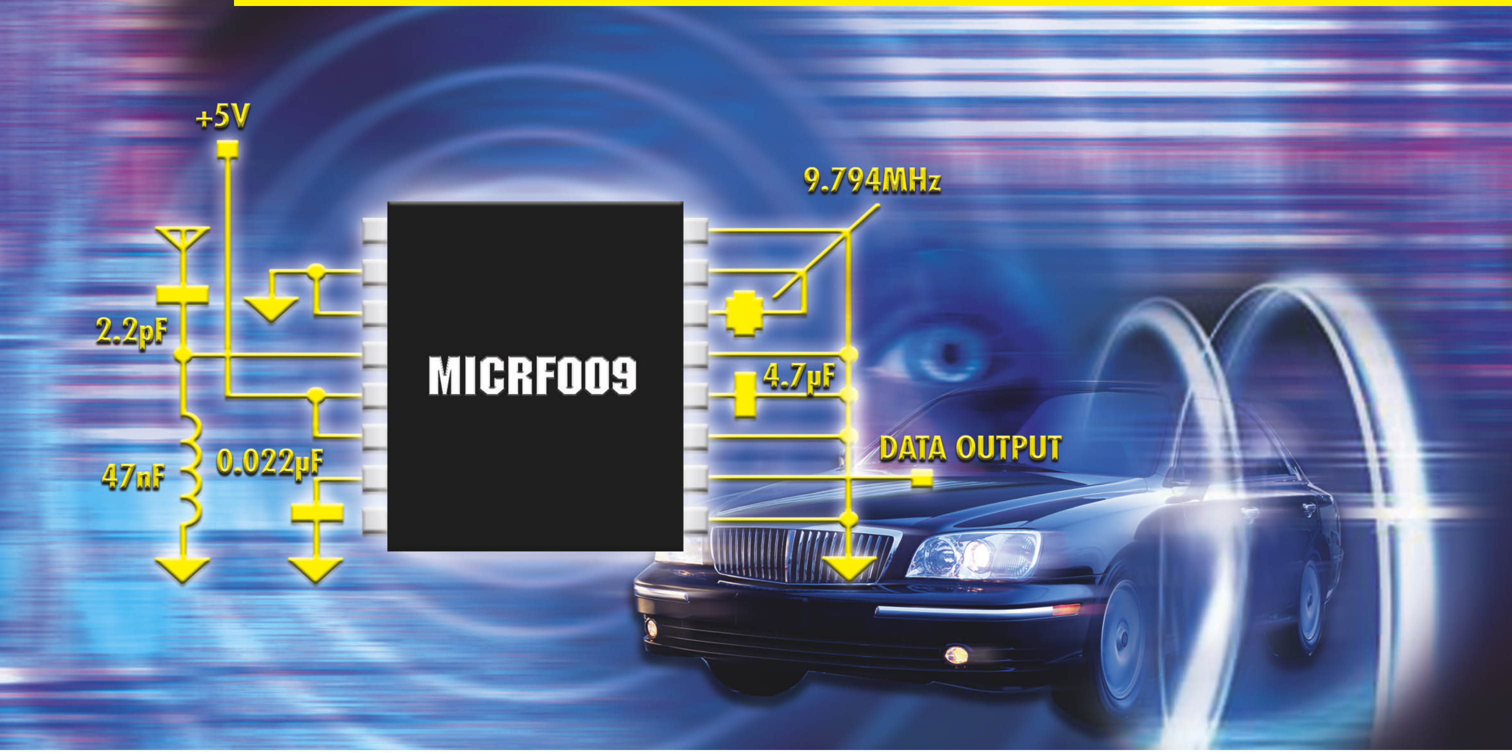
Page 69

STACKED-CHIP-SCALE-PACKAGE-DESIGN GUIDELINES

Page 79

More Value, Less Fuss.
RF Design Made Simple. No, Really.

QwikRadio® RF Receiver High Sensitivity, Fast Startup and Low Parts Count



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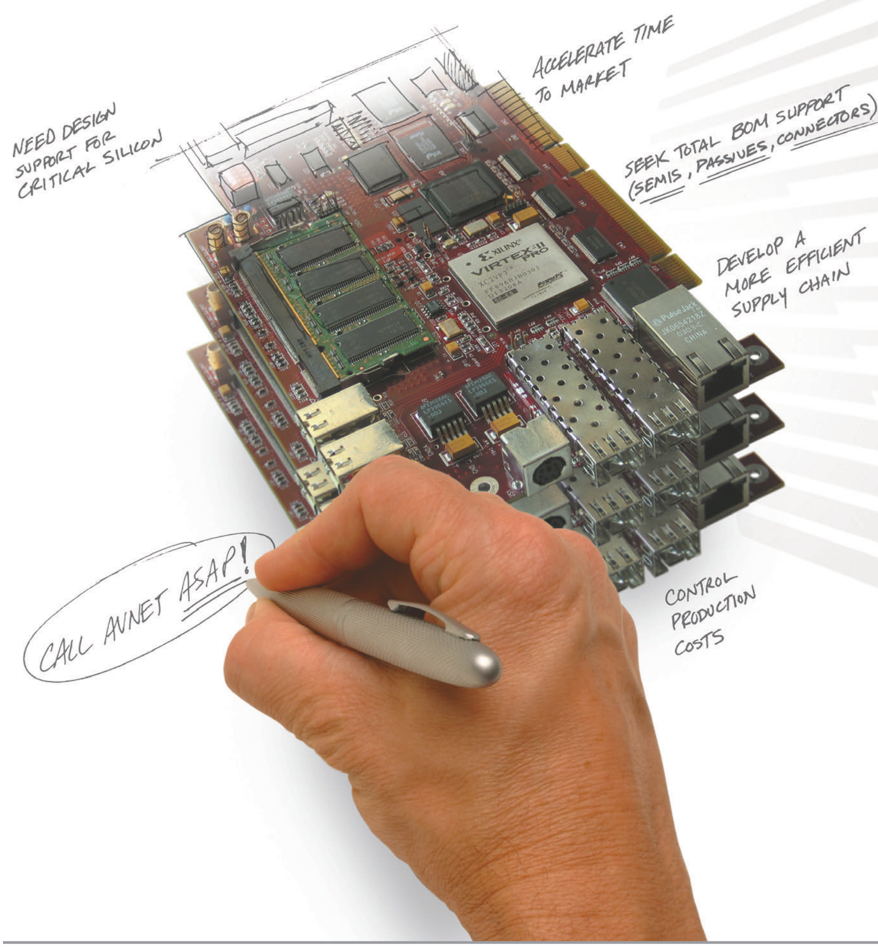

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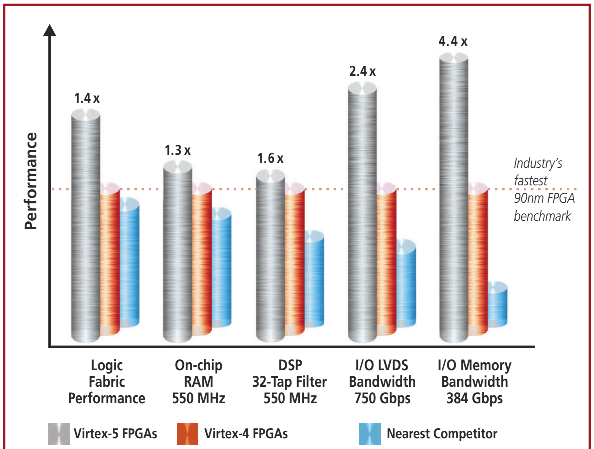

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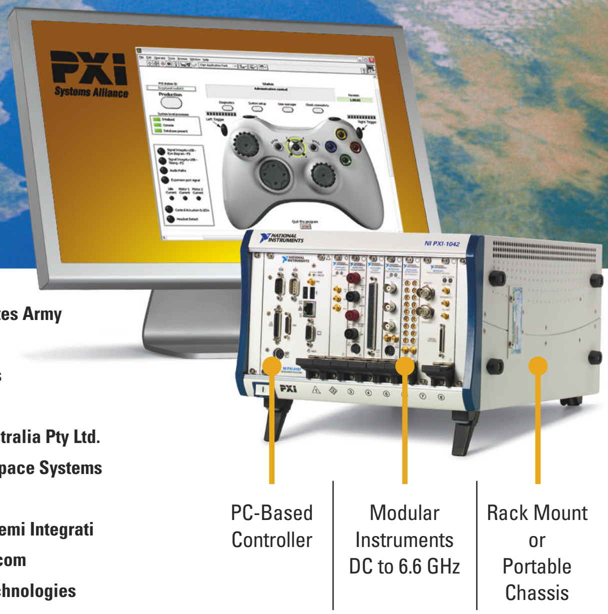

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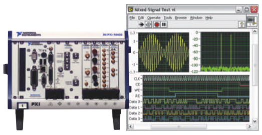

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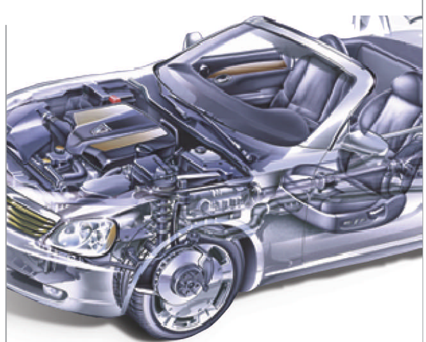
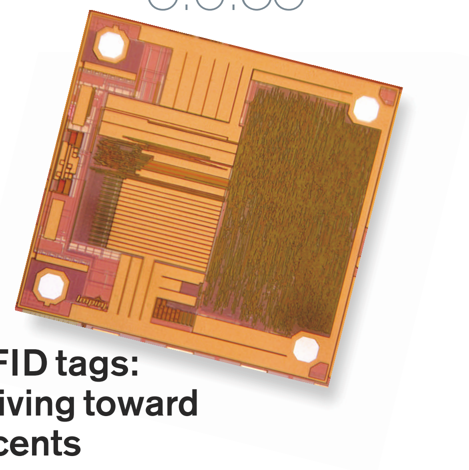
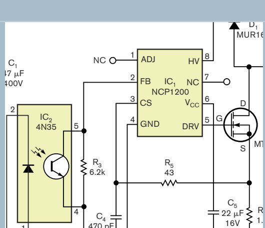




DESIGNIDEAS



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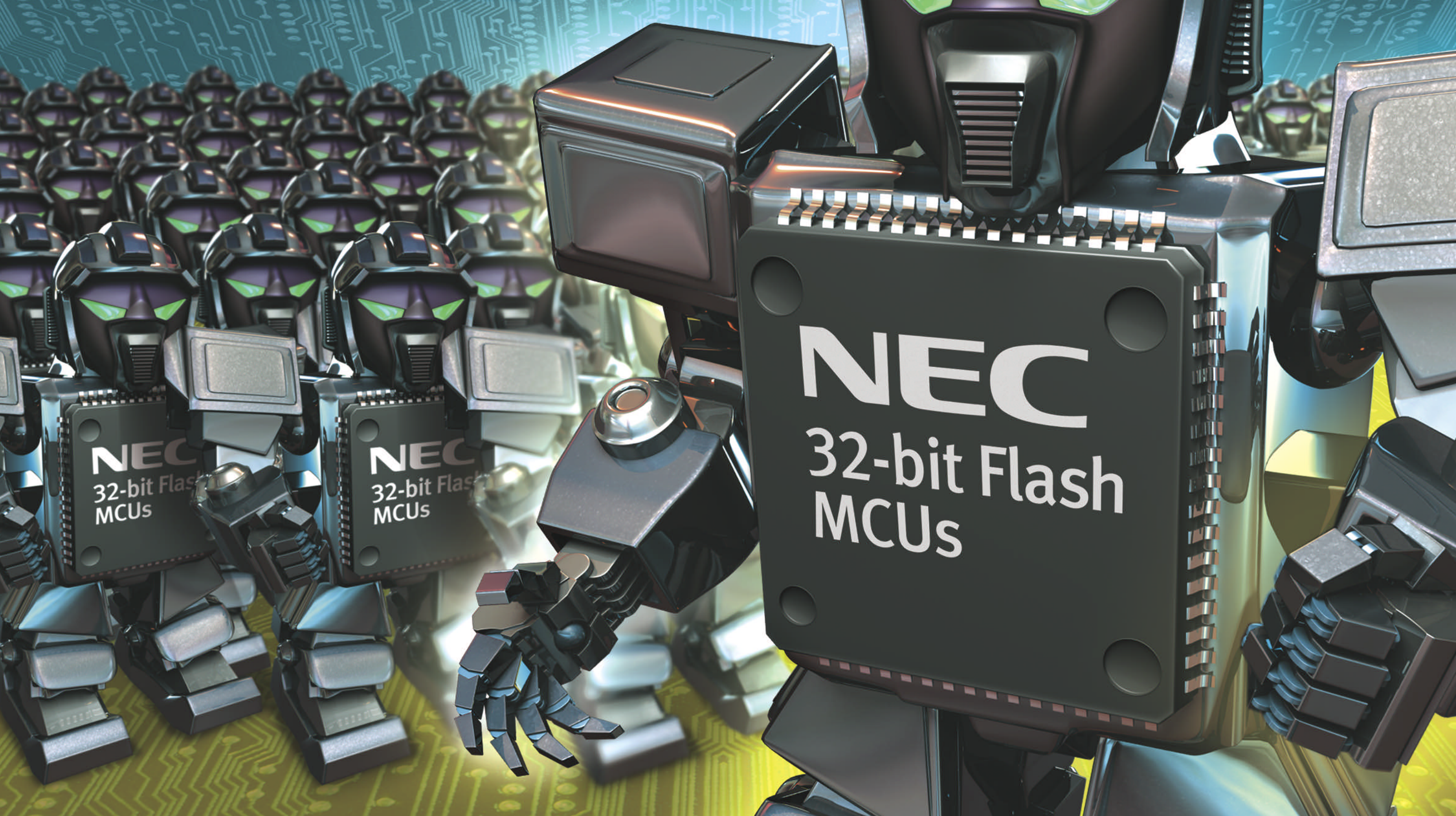

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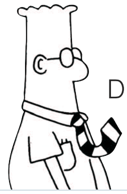
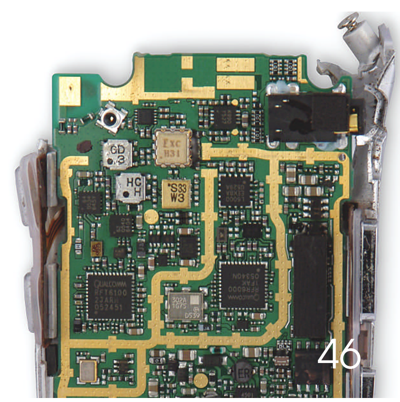


32

38



46

DEPARTMENTS & COLUMNS

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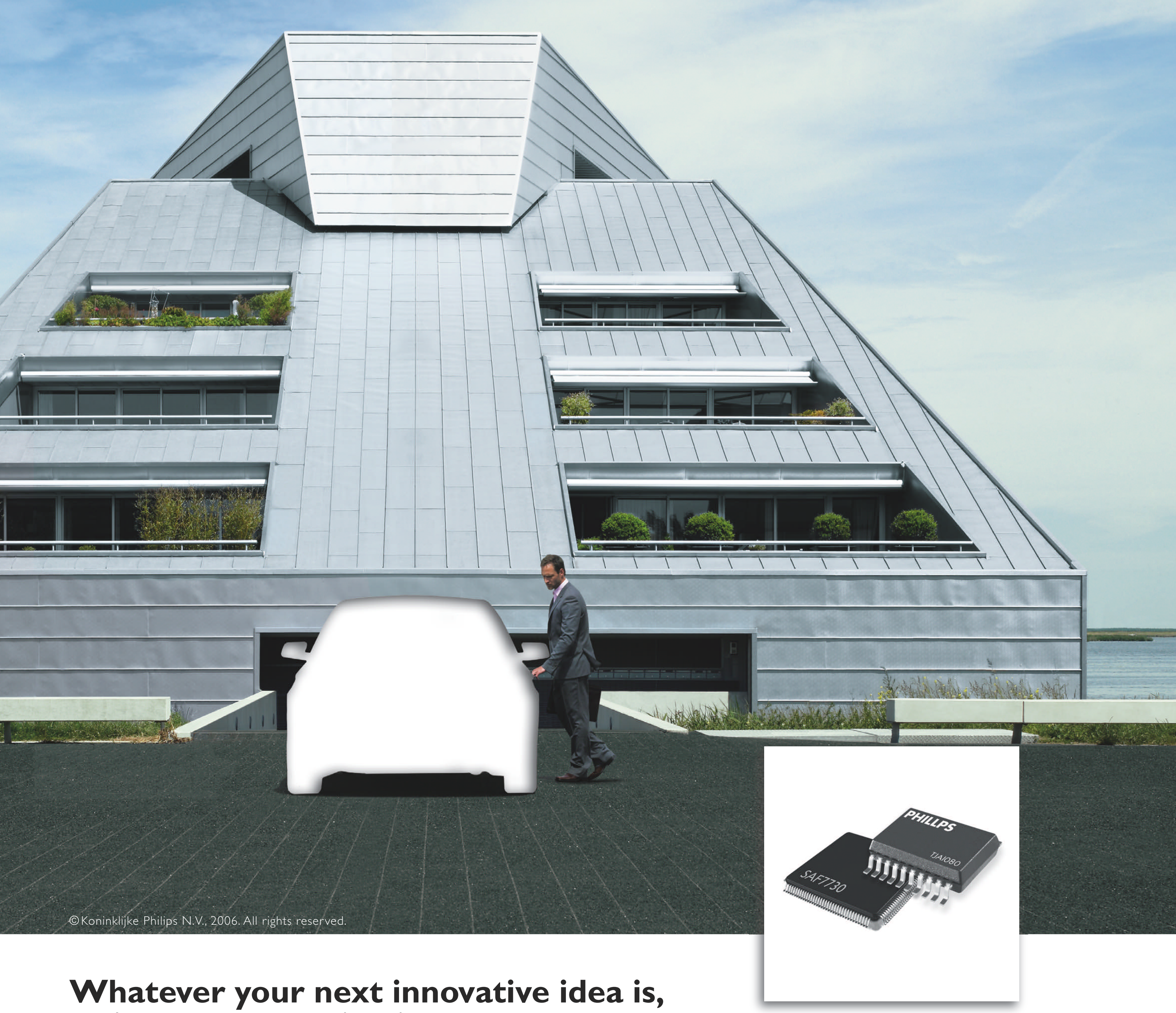
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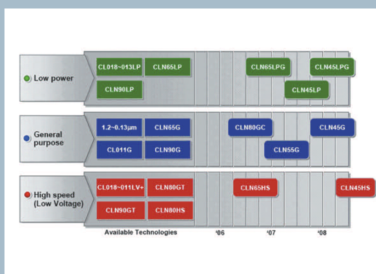

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READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

Designers cast a skeptical eye on mixed-signal SOCs
The functions are necessary, but integration challenges keep analog IP out of the mainstream for SOC design.
→ www.edn.com/article/CA6330094

Baker's Best: Charge your SAR-converter inputs
It is tempting to drive a SAR (successive-approximation register) ADC with just an amplifier. However, did you think about whether you would compromise the effectiveness of your op-amp/converter pair?
→ www.edn.com/article/CA6330093

Design Idea: JFET cascode boosts current-source performance
A constant-current source minimizes the reference circuit's sensitivity to supply-voltage fluctuations and extends the voltage reference's operating voltage beyond its 5.5V maximum rating.
→ www.edn.com/article/CA6330095

Fabless-ASIC company tries new model
Maybe the world isn't beating the bushes to find another fabless-ASIC company. But start-up Key ASIC believes that it has a model—an application-specific approach—that's just different enough to make a place for itself beside the relative giants.
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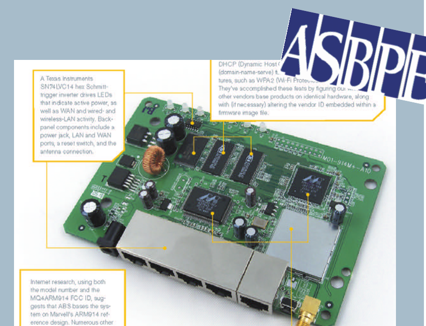

AWARDS

EDN RECENTLY WON THREE NATIONAL AWARDS FROM THE ASBPE
The American Society of Business Publication Editors (ASBPE) honored us with wins in three categories. Follow the links below to see our winning entries.

Best regular department (Prying Eyes):
→ www.edn.com/article/CA629314

Best redesign issue (June 9, 2005):
→ www.edn.com/toc-archive/2005/20050609.html

Best computer-generated cover art (Aug 18, 2005):
→ www.edn.com/article/CA633440

FROM THE VAULT

Articles and extras from the EDN *archives relating to this issue's contents.*

FPGAs BALANCE LOWER POWER, SMALLER NODES DRIP BY DRIP (pg 58):
Heat wave: FPGAs confront increasing, evolving power consumption
→ www.edn.com/article/CA438310
Low-power FPGAs target portable market
→ www.edn.com/article/CA6281905

STACKED-CHIP-SCALE-PACKAGE-DESIGN GUIDELINES (pg 79):
Rework within your reach
→ www.edn.com/article/CA447009

CHOOSING ANTIALIASING-FILTER AMPLIFIERS (pg 44):
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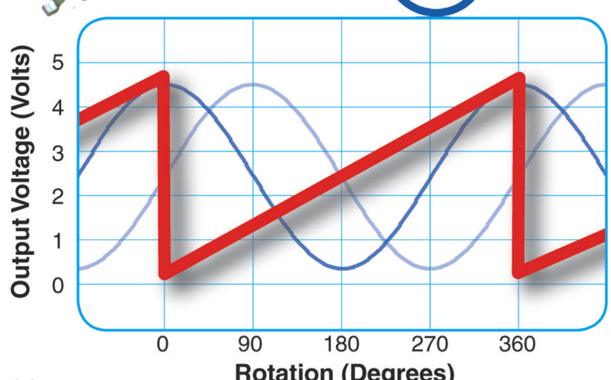

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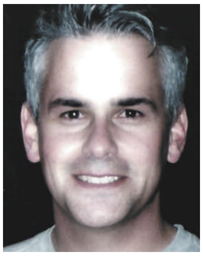

BY MICHAEL SANTARINI, SENIOR EDITOR

Spare us the drama, please

Cadence Design Systems late last month announced an ambitious and seemingly noble effort to create a common format so that tools throughout the design flow could share common data on power management. I've covered a number of EDA "standards efforts," and they tend to have more hidden agendas, back stabbings, and melodrama than the cheesiest soap operas. Eventually, the industry achieves its goals but typically not without months or years of delay due to unnecessary drama.

This initiative is tackling a crucial, time-sensitive problem. It's certainly no secret that low power—especially as it concerns leakage and heat—is becoming a bigger issue each time the industry moves toward finer process geometries. But power problems have become so bad that folks such as IBM's (www.ibm.com) Chief Technology Officer Bernard Meyerson have said that CMOS has now reached the peak level of modular heat flux (watts/centimeters squared) that made the industry drop bipolar technology as the mainstream-IC-design material in the late 1970s.

At the time, CMOS had several undesirable characteristics, but the industry adapted it anyway because of one huge advantage: CMOS was much lower powered than its bipolar counterpart.

Meyerson's presentation on the subject at the Global Press Summit in Monterey, CA, in February shows that a common household steam iron uses approximately $5W/cm^2$. Bipolar technology reached its peak at $14W/cm^2$ and then went the way of wafer-scale integration. According to Meyerson's presentation, CMOS today has also reached $14W/cm^2$.

But Cadence executives point out that, this time, the industry has no new, super-low-power silicon process to easily adopt. So, the IC-design chain has to figure out a way to stretch the life of CMOS and find ways to manage power and heat. Foundries and equipment makers are working to reduce power and heat on their new CMOS processes by adopting thicker oxide transistors, low-power libraries, SOI (silicon-on-insulator) technology, and MTCMOS (multithreshold CMOS).

About four years ago, EDA companies, most notably Apache Design Solutions (www.apache-da.com), foresaw the problem and introduced tools. At the last Design Automation Conference in June 2005 in San Francisco, almost a dozen EDA vendors offered power tools. Most of these tools deal with power at the back end of the design process, during physical design and analysis. And so far, only one EDA vendor, Gradient Design Automation (www.gradient-da.com), deals with on-chip thermal technology.

Now, Cadence's (www.cadence.com) "Power Forward" initiative aims to derive a common power format that allows tools at the front of the design process—at the RTL and even higher at the chip architectural level—to share power data with back-end tools, libraries, and perhaps even manufacturing.

But Cadence is really not the first company most folks think of when the topic of low-power design tools pops up. Cadence does, however, have a lot of pull, because it is the largest EDA company and seemingly has the largest ASIC-designer user base.

Cadence has put a real go-getter on the job. Chi-Ping Hsu, the technology brain behind Avanti, which Synopsys (www.synopsys.com) now owns, and the former chief executive officer of Get2Chip, which Cadence acquired, is organizing the technical effort.

What's bound to make some folks cringe and dust off the old soapboxes is that Cadence isn't initially consulting with any other EDA vendors to create the format—not even Apache. The company has, however, signed on with ARM (www.arm.com), NEC (www.nec.com), TSMC (www.tsmc.com), Applied Materials (www.appliedmaterials.com), AMD (www.amd.com), ATI (www.ati.com), Freescale (www.freescale.com), and Fujitsu (www.fujitsu.com) to be its "power-forward advisors"; these companies will donate time and effort to help Cadence create the CPF (common power format).

Cadence claims it isn't inviting any other EDA companies to help during the format-devising stage so the company can prevent the too-many-cooks-in-the-kitchen phenomenon and can quickly create a basic working format. But Cadence expects that, in early 2007, it will open its "power-forward general membership" and invite other EDA companies to adopt the format and quickly make changes. It would be nice for a change to report that the EDA industry has matured and accelerated the adoption of a standard for the greater good of its customers and the industry and that it has created a de facto standard and not just another IEEE-approved standard. It would also be nice for a change to report on a standard that the industry adopts because it is fair, comprehensive, and open and not simply because Cadence's muscle dictates that it's a standard. EDN

Contact me at michael.santarini@reedbusiness.com.

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No. 112

Synchronous Rectification in High–Performance Power Converter Design

— By Robert Selders, Jr., Applications Engineer

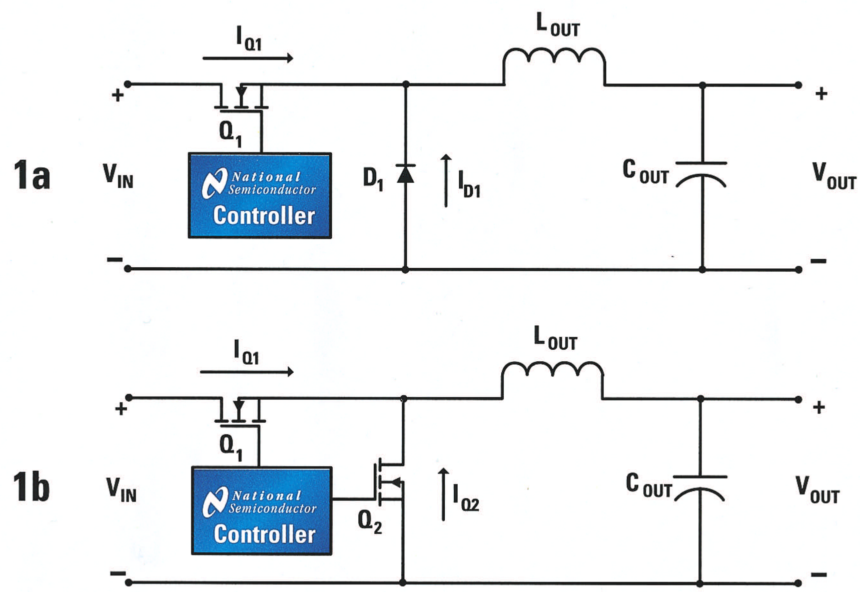

Figure 1. (a) Non-synchronous and (b) Synchronous Buck Converters

Power converters are becoming increasingly commonplace in the electrical industry. Product manufacturers and suppliers of electrical equipment are demanding ever-increasing functionality (i.e., lower input and output voltages, higher currents, faster transient response) from their power supply systems.

To meet these demands, switching power supply designers in the late 1990s began adopting Synchronous Rectification (SR)—the use of MOSFETs to achieve the rectification function typically performed by diodes. SR improves efficiency, thermal performance, power density, manufacturability, and reliability, and decreases the overall system cost of power supply systems. This article will examine the advantages of SR and discuss the challenges encountered in its implementation.

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LED Backlighting Applications

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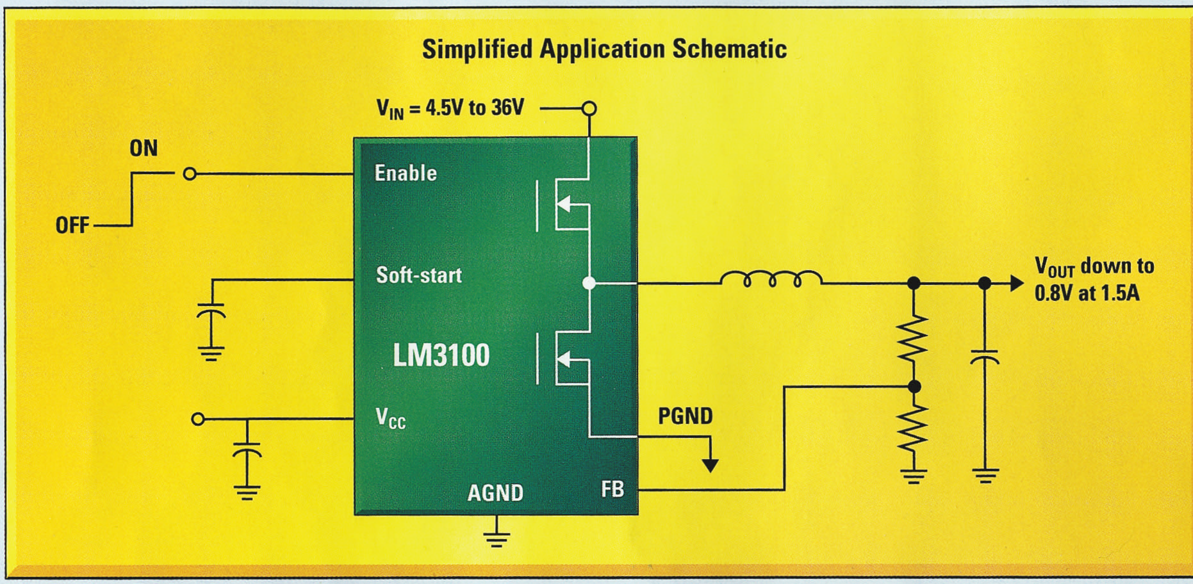

LM3100 Features

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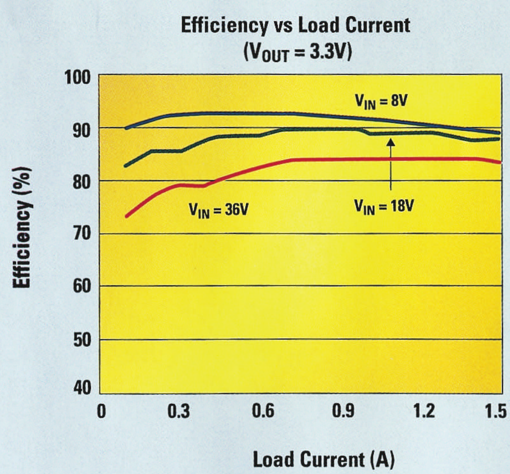

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Synchronous Rectification in High-Performance Power Converter Design

Drawbacks of Diode Rectification

Nonsynchronous and synchronous buck converters are shown in *Figure 1*. A nonsynchronous buck converter uses a FET and Schottky diode as its switches *(Figure 1a)*. When the FET turns on, energy is delivered to the output inductor and the load. When the FET turns off, the current in the inductor commutates to the Schottky diode. Provided the load current is higher than half the ripple current of the output inductor, the converter operates in the continuous conduction mode.

The Schottky diode is selected by its forward voltage drop and reverse leakage current characteristics. But as output voltages drop, the diode's forward voltage is more significant which reduces the converter's efficiency. Physical limitations prevent the forward voltage drop of diodes from being reduced below approximately 0.3V.

In contrast, the on resistance, R_{DSON}, of MOSFETs can be lowered, either by increasing the size of the die or by paralleling discrete devices. Consequently, a MOSFET used in place of a diode can have a significantly smaller voltage drop at a given current than the diode.

This makes SR attractive, especially in applications sensitive to efficiency, converter size, and thermal performance, such as portable or handheld devices. MOSFET manufacturers are constantly introducing new MOSFET technologies that have lower R_{DSON} and total gate charge, (Q_G), which makes it easier to implement SR in power converter design.

What is Synchronous Rectification?

In the synchronous buck converter, for example, the efficiency is increased by replacing the Schottky diode with a low side MOSFET *(Figure 1b)*. The two MOSFETs must be driven in a complimentary manner with a small dead time between their conduction intervals to avoid shoot–through. The synchronous FET operates in the third quadrant, because the current flows from the source to the drain. In contrast to its nonsynchronous counterpart converter, the synchronous buck converter always operates in continuous conduction, even down to no load.

During the dead time periods, the inductor current flows through the lower FET's body diode. This body diode usually has a very slow reverse recovery characteristic that can adversely affect the converter's efficiency. An external Schottky diode can be placed in parallel with the low-side FET to shunt the body diode and prevent it from affecting the converter's performance. The added Schottky can have a much lower current rating than the diode in a nonsynchronous buck converter because it only conducts during the small dead time (which is typically less than a few percent of the switching cycle) when both FETs are off.

Benefits of Synchronous Rectification

The advantages of using SR in high-performance, high-power converters include better efficiency, lower power dissipation, better thermal performance, lower profile, increased quality, improved manufacturing yields though automated assembly processes (higher reliability), and inherently optimal current sharing when synchronous FETs are paralleled.

As mentioned above, a number of MOSFETs can be paralleled to handle higher output currents. Because the effective R_{DSON} in this case is inversely proportional to the number of paralleled devices, conduction losses are reduced. Also, the R_{DSON} has a positive temperature coefficient so the FETs will automatically tend to share current equally,

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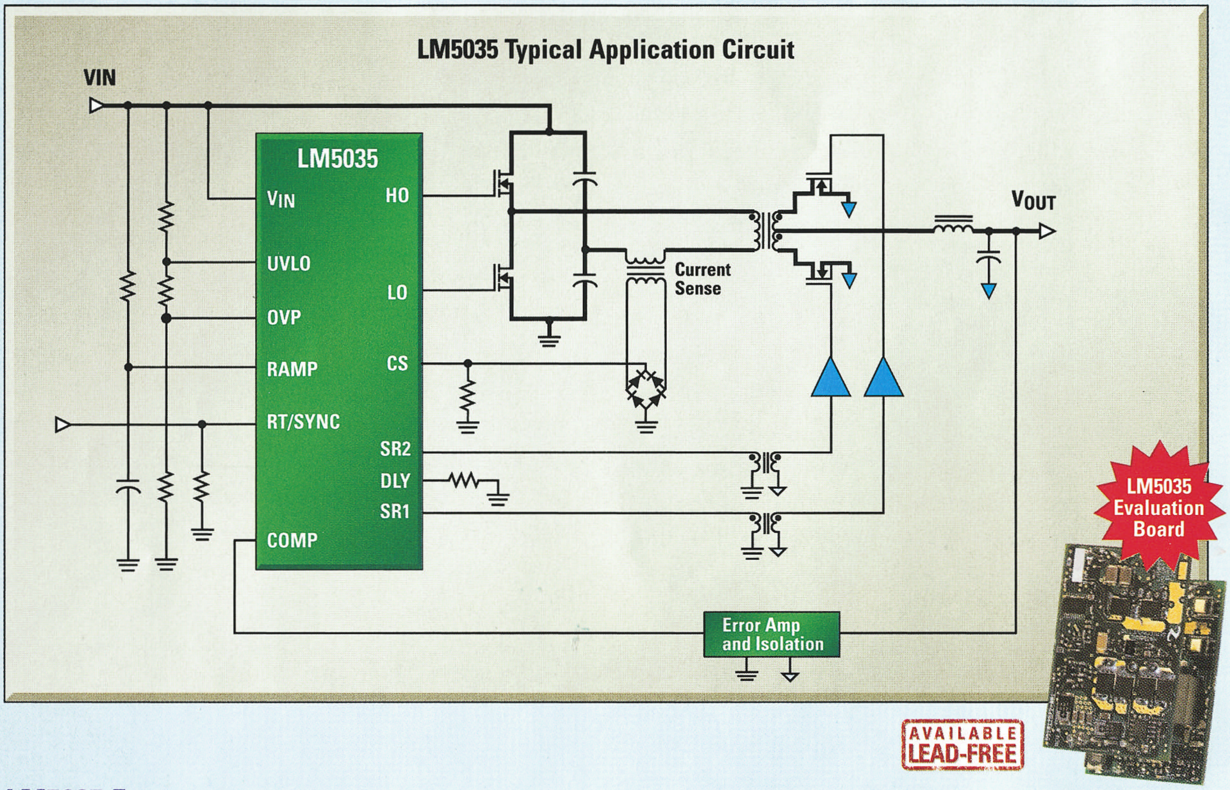

LM5035 Features

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Synchronous Rectification in High Performance Power Converter Design

facilitating optimal thermal distribution among the SR devices. This improves the ability to remove heat from the components and the PCB, directly improving the thermal performance of the design. Other potential benefits from SR include smaller form factors, open frame configurations, lower profiles, higher ambient operating temperatures, and higher power densities.

Design Trade-Offs in Synchronous Rectified Converters

In an effort to minimize the size of the converter and decrease output ripple voltage for low-voltage applications, designers often increase the switching frequency to reduce the size of the output inductor and capacitor. If multiple FETs are paralleled, this increase in frequency can also increase gate drive and switching losses.

Design trade-offs must be made on a per-application basis. For example, in a high input voltage, low output voltage synchronous buck converter, since the operating conditions are such that the high-side FET has a significantly lower RMS current than the low-side FET, the high-side FET should be chosen with less Q_G and higher R_{DSON}. It is more critical to lower switching losses for this device than conduction losses. Conversely, the low-side FET carries more RMS current so its R_{DSON} should be as low possible.

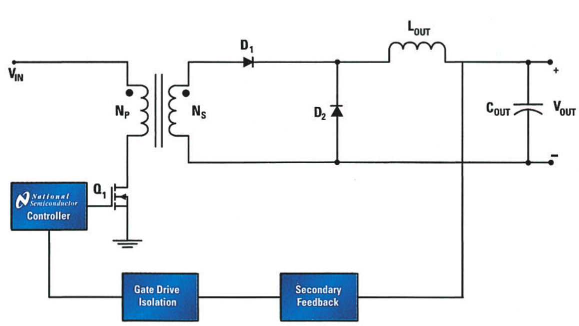

Figure 2. Isolated power converter with output synchronous rectification

Selecting controllers with stronger gate drivers in synchronous converters reduces switching losses by minimizing the time the FETs take to switch. However, faster rise and fall times generate high frequency noise that can lead to system noise and EMI compliance issues.

Driving Synchronous Rectifiers in Isolated Topologies

Power converters utilizing isolated topologies are used in systems requiring galvanic isolation among system grounds. Such systems include distributed bus architectures, Power-over-Ethernet systems, and wireless basestations. *(Figure 2)*.

Using SR in isolated converters can improve their performance significantly. All isolated topologies: forward, flyback, push-pull, half and full bridge (current and voltage fed), can be synchronously rectified. However, providing adequate and well-timed gate drive signals to the SRs in each topology presents its own set of challenges.

There are basically two types of drive schemes for FETs on the secondary stage of isolated topologies: self-driven gate signals taken directly from the secondary transformer windings, and control-driven gate signals derived from the PWM controller or some other primary referenced signal. For a given application several different implementations of these drives are possible. The designer should choose the simplest solution that also meets the performance requirements.

The self-driven scheme is the simplest, most straight forward SR drive scheme *(Figure 3)* and works well in topologies where the transformer

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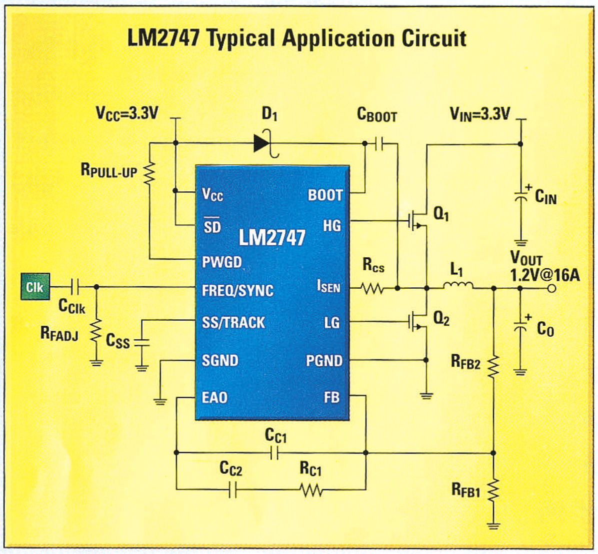

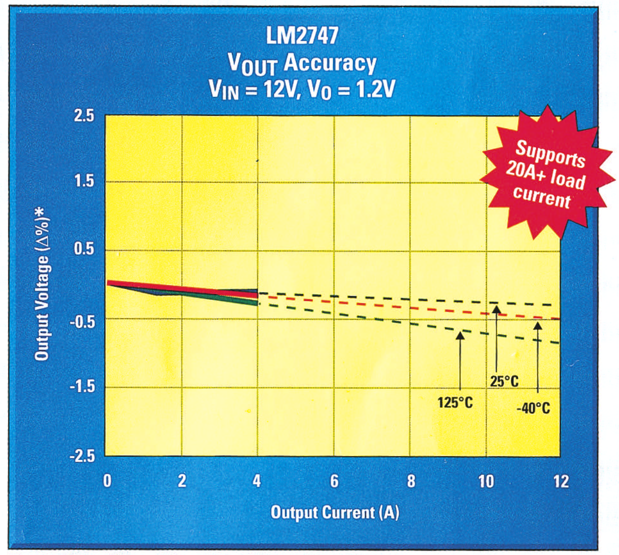

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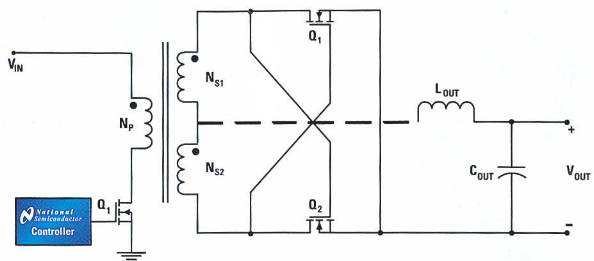

Figure 3. Self-driven synchronous rectification output stage

voltage is not zero for any significant period of time. Two SR FETs replace the output rectifier diodes, and voltage generated across the secondary windings drives the gates of the SRs. In most cases, higher or lower output voltages can be achieved with same topology by utilizing a different transformer turns ratio (N_P:N_{S1}:N_{S2}) and by appropriately selecting the SR FETs.

The main problem with self-driven SRs in topologies where the transformer voltage periodically goes to and stays at zero is that there is no signal to drive the gates of the SR FETs during these intervals. During these times, body diodes of the SRs conduct the load current, thus increasing power losses. Lower output voltages may require additional windings to increase the normal operating voltage applied to the SR FET gates to an adequate level.

Because the secondary winding voltage varies with input line voltage, the voltage on the SR gates will vary. The efficiency is impacted because R_{DSON} depends on the gate-source voltage (V_{GS}). In wide input voltage range converters this R_{DSON} variation can be as high as 2:1.

There are alternate gate drive techniques that can be employed for transformer-based topologies. In low-voltage, high-current applications, these drive techniques both reduce losses associated with the dead time intervals and produce nearly constant-amplitude gate drive pulses so efficiency is not adversely impacted by varying line voltages.

Control-driven schemes tend to solve the limitations of self-driven methods. However, they are typically more complex and expensive ***(Figure 4)***. Depending on how parts-intensive the self-driven scheme is, a control-driven scheme may actually be the better alternative. The control signals used to drive the SR FETs can be derived from a primary or secondary side referenced controller.

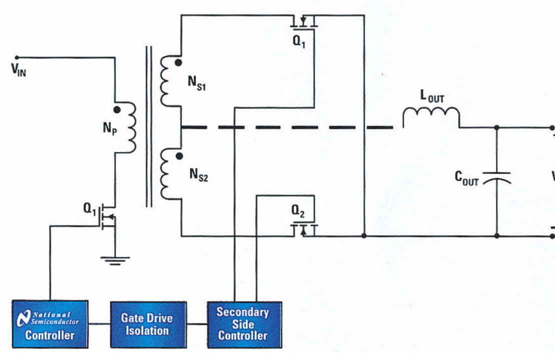

Figure 4. Control-driven synchronous rectification output stage

Conclusion

Synchronous switching power converters give better performance than nonsynchronous converters in low output voltage, high output current systems applications. Ensuring the proper timing of the gate drive signals for the SRs is an important task that designers must address to maximize converter performance. ■

Acknowledgement: The author would like to thank Dr. Haachitaba Mweene for his feedback on the article.

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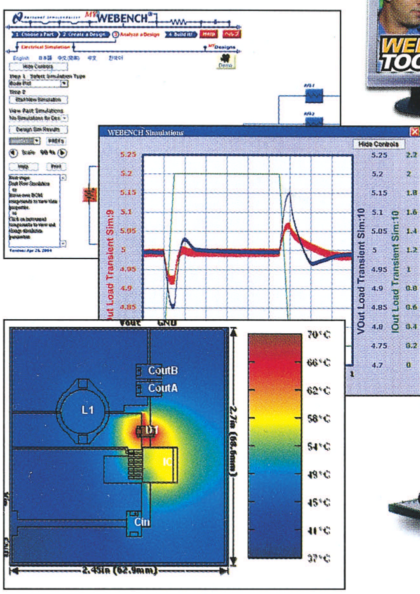

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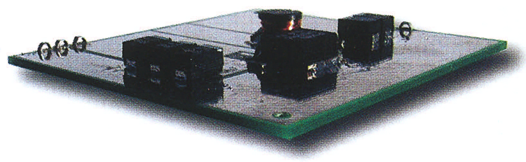

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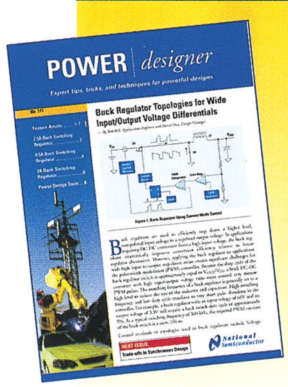

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INNOVATIONS & INNOVATORS

Mesh networks publish remote data

A new mesh-sensor network from Accsense features an Internet gateway and as many as 16 wireless pods that deliver remote process measurements to any Web-enabled device.

Claiming to offer the modern replacement for the venerable strip-chart recorder, Accsense recently introduced a wireless-sensor system that measures a wide range of physical properties and delivers real-time data to any Web-enabled device. The company based the system on wireless-sensor pods that measure ambient temperature, humidity, light, noise, and vibration and automatically form a secure, self-healing wireless-mesh network with a range as long as 4000 ft. Accsense sensor pods are compatible with a range of standard external plug-in sensors and probes, including thermocouples, resistance-temperature detectors, and thermistors.

A complete Accsense system includes as many as 16 wireless-sensor pods, a Pod Gateway for connecting the sensor network to the Internet, and an online account for monitoring, storing, and analyzing data. Sensor pods range in price from $295 to $635, depending on the combination of measurements and number of inputs. The Pod Gateway sells for $795 and supports as many as 16 pods. The Accsense-hosted online service is available through a monthly subscription. The standard account is free and enables users to monitor their data online and download it for deeper analysis. At $24.95 per month, the premium account offers additional features, such as analytical charting and alarms that send alerts to cell phones, pagers, and e-mail if measurements fall out of range.**—by Warren Webb**

▷**Accsense Inc**, www.accsense.com.

FROM THE VAULT

"More than ever before and certainly without challenge today in light of sagging aerospace and defense programs, expenditures, and sentiment, the information-processing industries are sure to be the darling of the '70s. In 1970, the nearly all-pervasive computer will take great strides toward becoming all-pervasive. Communications with the computer and communications between computers will expand old opportunities and create limitless new opportunities."

Jerry Sanders, President, AMD, *EDN*, Jan 1, 1970

PWM controllers drive Intel dual-core processors

Pentium-class processors offer among the toughest challenges for power-system designers, and the new dual-core chips that meet the Intel VR11 power spec are no exceptions. Intersil is attacking the VR11 market with a controller that can use four to six synchronous-rectified buck channels in parallel. Transient response is a huge problem for such power subsystems.

The new Intersil ISL6326 and ISL6327 controllers rely on the company's active-pulse-positioning and adaptive-phase-alignment technologies to speed response to load transients, thereby reducing the requirement for external bulk capacitors. A differential amplifier remotely senses voltage, eliminating any potential difference between remote and local grounds, thereby improving regulation and accuracy. Prices for the controllers range from $3.81 to $4.58 (1000).

—by Maury Wright

▷**Intersil**, www.intersil.com/power.

With adjustable switching frequency as high as 1 MHz per phase, the ISL6326 and ISL6327 PWM controllers meet the Intel VR11 spec.

ARM9 microcontroller touts connectivity, large on-chip memory

STMicroelectronics' STR-910F series of ARM-9E-based microcontrollers combine Ethernet, CAN (controller-area-network) 2.0B, and USB-FS support; as much as 96 kbytes of SRAM; and as much as 544 kbytes of flash in a single device. The ARM9E core includes single-cycle DSP instructions that can take advantage of simultaneous access of code and data. The core operates at 1.8V±10%, and the I/O ring operates at 2.7 to 3.6V. The burst flash supports a minimum of 100,000 erase cycles with 20-year data retention, and it can support a peak execution performance of 96 MHz.

The Ethernet MAC (media-access controller) includes an MII (media-independent interface) to an external PHY (physical) layer. The dedicated Ethernet DMA controller can support the movement of 91 Mbps of raw Ethernet frames between the MAC and the SRAM while loading the CPU by 10%. Other peripherals include an eight-channel, 10-bit ADC; a three-phase ac-motor-control unit; supervisor functions with low-voltage-reset and brownout detection; a real-time clock; and as many as 80 5V-tolerant I/O pins.

The core and peripherals access the SRAM through an alternating arbiter that guarantees a deterministic, direct path to the SRAM. The real-time clock draws less than 1 µA across the entire temperature range. It can record the time of a tampering event and cut power to the SRAM to destroy contents if desired; external real-time-clock devices costing 50 cents to $1 each typically support these features. Power consumption of the core ranges from 1.3 mA/MHz in run mode to 55 µA in sleep mode, in which the device is quiescent with the real-time clock running. Battery current when the main power is off with only the real-time clock operating is as low as 0.3 µA at room temperature and 0.9 µA maximum, and it is 5 µA at room temperature and 85 µA maximum when the SRAM is also alive.

Six STR910F devices are available now in lead-free packages with prices starting at $6.99 (10,000). The LQFP-80 and LQFP128 packages support operation over a temperature range of −40 to +85°C. The LQFP128 packages include an Ethernet MII and an external-memory-bus interface. Starter kits are available from Hitex (www.hitex.com), IAR Systems (www.iar.com), Keil Software (www.keil.com), and Raisonance (www.raisonance.com) for as low as $199. These kits include free compilers that are code-limited to either 16 or 32 kbytes. The kits also include JTAG debugging, programming cable, code examples, and hardware to begin a design.

> The CAPS tool allows developers to configure I/O-pin and clock functions using a graphical interface.

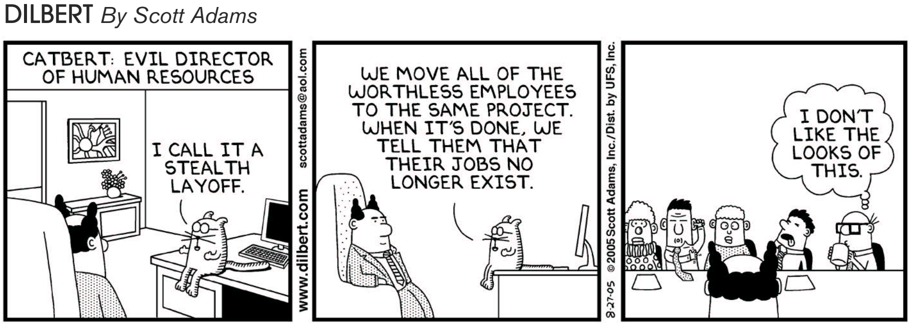
The STR910F series of ARM9E-based microcontrollers combine Ethernet, CAN 2.0B, and USB-FS support; as much as 96 kbytes of SRAM; and as much as 544 kbytes of flash.

The $249 STR910-Eval evaluation board allows designers to exercise and evaluate all of the hardware interfaces and I/O of the STR-910F. Designers can use the included demonstration code for the Ethernet, USB, CAN, and other major chip functions based on a common HAL (hardware-abstraction-layer) library. STMicroelectronics' free CAPS (configuration-and-programming-software) tool allows developers to configure I/O-pin and clock functions using a graphical interface. The tool automatically generates a C header file that reflects the developer's pin and clock choices. RTOS and TCP/IP support are available from CMX (www.cmx.com), Micrium (www.micrium.com), Segger (www.segger.com), Keil, and NexGen Software (www.nexgen-software.fr/PublicAsp).

—by Robert Cravotta

▷**STMicroelectronics**, www.stm.com.

DILBERT *By Scott Adams*



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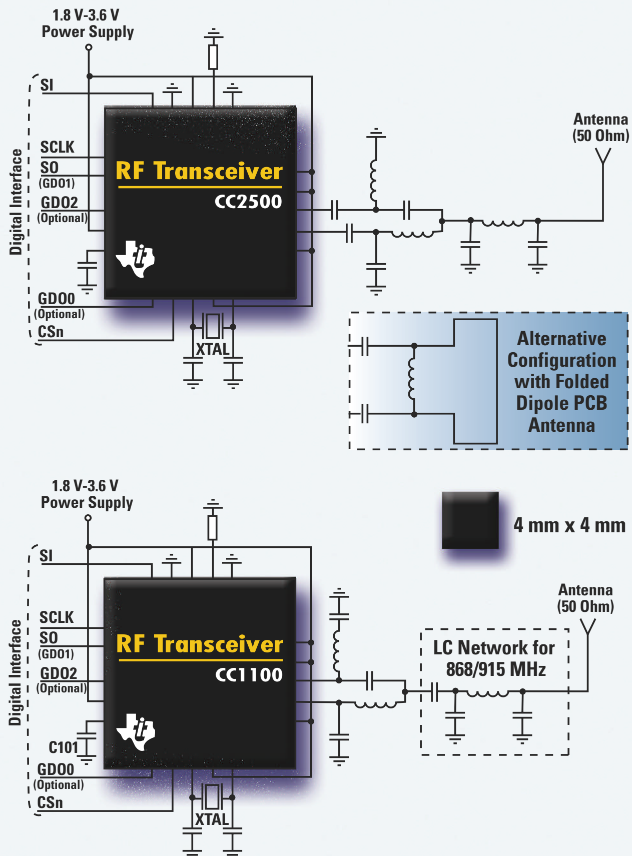

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Logic analyzers sport 32M-sample memory

Agilent Technologies has expanded its logic-analyzer portfolio with eight new fixed-configuration models that constitute its next-generation 16800 series. The Agilent 16800 family of analyzers offers high-performance measurement capabilities in a small, fixed-configuration package with advanced features at affordable prices. Each model in the family comes with a 15-in. display and optional touch-screen interface. This interface has for more than 20 years been a hallmark of Agilent's modular-logic-analyzer systems but has never before been available in a fixed-configuration model. Touchscreen capability offers fast, intuitive interaction and works well when limited bench space hinders the use of a mouse and a keyboard.

The analyzers quadruple the industry's maximum fixed-configuration-memory depth to 32M samples. This acquisition depth was previously available only in higher priced modular logic analyzers. In addition, three models offer an integrated digital stimulus that allows design teams to quickly emulate missing components, inject faults, and perform design characterization.

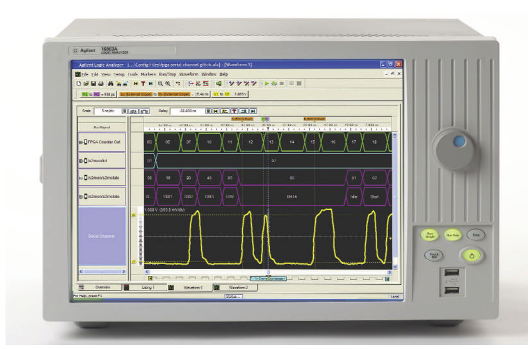
All models, ranging from 34 to 204 channels, provide 4-GHz timing sampling with 250-psec resolution simultaneously with state measurements, eliminating the need to double-probe. Unique in the industry, the models allow for independent installation of upgrades in acquisition-memory depth and state speed—but not channel count—enabling development teams to purchase what they need today at a lower price and to upgrade memory depth or state speed as their needs grow. For example, 16800 users can start with a system configured for 250-MHz state speed and 1M-sample acquisition depth; as their needs grow, they can upgrade to 450-MHz state speed and as much as 32M-sample acquisition depth.

"For the first time, design teams that purchase fixed-configuration logic analyzers have access to advanced capabilities previously found exclusively in more expensive modular systems," says Sigi Gross, general manager of Agilent's Digital Verification Solutions division. He says that feedback from Agilent customers highly influences the 16800 series' usability and features. "We focused on delivering important new capabilities and great usability at an affordable cost," says Gross. The familiar Microsoft Windows XP Pro user interface helps new users to quickly become productive.

Prices for 16800-series logic analyzers start at $9430 for a 34-channel unit. A 48-channel pattern generator, available in analyzers that have as many as 102 logic-analysis channels, adds $8000. Prices for groups of 34 additional logic-analysis channels start at approximately $2200 per group. A 204-channel logic analyzer costs $25,000.

—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/16800.



A clean front panel and a huge display are hallmarks of the 16800 series of fixed-configuration logic analyzers, which allow memory depths to 32M samples/channel, state-analysis speeds to 450 MHz, and timing-analysis resolution to 250 psec.

FROM THE VAULT

"The explosion in demand for ICs is greater than anyone had imagined. This demand will tax the world's capacity for development and production. Apart from the enormous growth in the data-processing market, consumer applications will represent a significant portion of this demand for ICs."

Edward Meagher, vice president of marketing, Amperex Electronics Corp, *EDN*, Jan 15, 1970

06.08.06

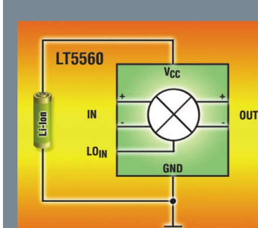
Agile mixer targets RFID, GSM, and WiMax

You can configure Linear Technology's new LT5560 as an upconverting or downconverting mixer, and it can serve in public-safety handheld radios, WiMax-transceiver modems, handheld RFID readers, VHF/UHF transceivers, GSM/EDGE (global-system-for-mobile-communications/enhanced-data-for-GSM-evolution) base stations and repeaters, and ISM (industrial/scientific/medical)-band radios.

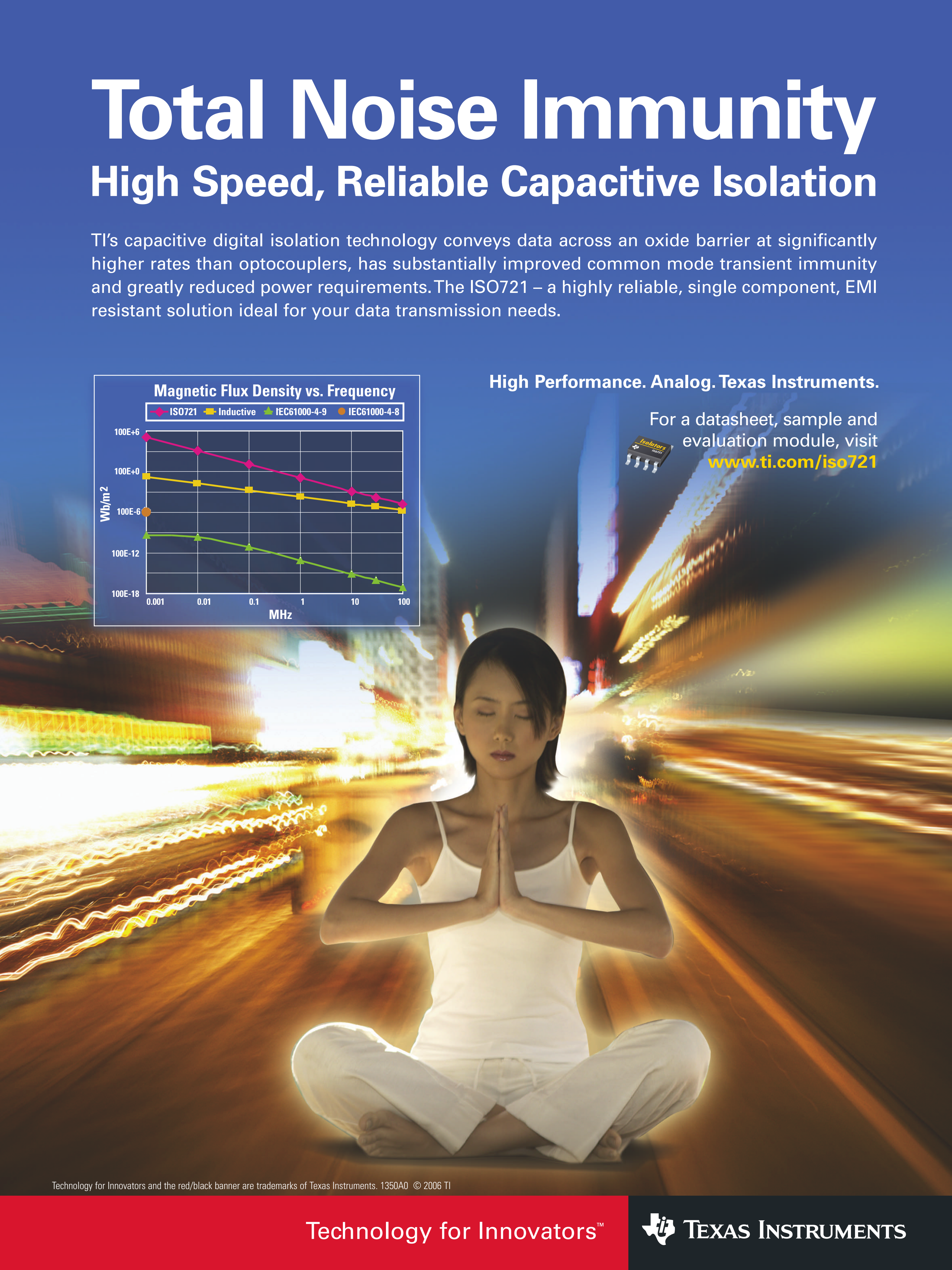
As a 900-MHz downconverting mixer with nominal supply current of 10 mA, the design yields a third-order-intercept-point spec of 9.7 dBm and a noise figure of 10.1 dB. Typical current consumption is 10 mA, although an external resistor can adjust current use to as little as 4 mA. A disable function reduces current draw to 0.1 μA in power-managed operation. Prices start at $1.56 (1000).

—by Maury Wright

▶**Linear Technology**, www.linear.com.



The LT5560 operates at 10 kHz to 4 GHz, integrates a double-balanced mixer core for maximum linearity and RF isolation, and operates from a 2.7 to 5.25V supply.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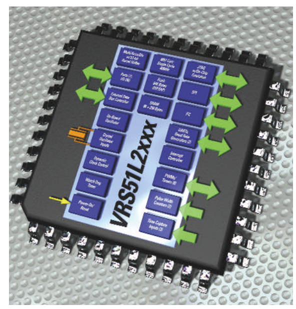
8051 core provides hardware-arithmetic extensions

Ramtron's VRS51L2070, the latest device in the Versa 8051 microcontroller family, integrates a single-cycle, 40-MHz, 8051-based core with 4 kbytes of SRAM; 64 kbytes of in-system- and in-application-programmable flash; a JTAG-programming/debugging interface; and digital-signal-processing extensions. The multiply/accumulate/divide unit includes a 32-bit barrel shifter that can perform single-cycle, 16-bit signed multiplication and 32-bit addition, and it can perform a 16-bit, signed division in five cycles. You access the multiply/accumulate/divide unit through the 8051's SFRs (special-function registers).

To lower costs of embedded-system designs, the VRS51L2070's internal oscillator supports 40-MHz operation with 2% accuracy. The device includes eight PWMs with 16-bit adjustable resolution. Two pulse-width counter modules enable event-duration measurement. The integrated SPI can support transactions as fast as 20 Mbps that are adjustable from 1 to 32 bits. Each UART incorporates a dedicated baud-rate generator with 16-bit resolution and 4-bit micro-baud-rate adjustment. Other peripherals include an I²C, three 16-bit timers/counters with three timer-capture inputs, a watchdog timer, and 49 interrupts that share 16 interrupt vectors. The VRS51L2070 is currently available for sampling and costs less than $4 (10,000) in a QFP-64 package.

—by Robert Cravotta

▷**Ramtron**, www.ramtron.com.



The VRS51L2070's internal oscillator supports 40-MHz operation with 2% accuracy.

Power-dense, 200W ac/dc supply feeds communication systems

Datacom and telecom centers, with their power-hungry banks of servers, place some of the highest power-density requirements on ac/dc-switching power supplies. To address these requirements, XP Power has introduced the 212W EMA212 in a 1U-compatible, 3×5×1.34-in. package. The company claims that the unit holds the power-density record for a 200W ac/dc-switching supply. Power density is 10.55W/in.^{3} at an efficiency of 91%. The unit's primary voltage rail is available across the entire input voltage range of 90 to 264V ac and temperature range of −10 to +50°C, with no derating for temperature. The supply has an auxiliary 12V, 1A fan output and a 5V standby at 100 mA for housekeeping. It requires 12 cfm forced-air cooling.

The supply's design relies on a variety of known power-supply-design techniques to achieve high power density. For example, the supply has a two-stage input filter with high-permeability-core chokes. XP stacks the chokes on top of the polypropylene capacitors in a technique that company officials believe is unique. "It saves us the pc-board real estate and brings the hot chokes up to pick up some of the airflow," says Mike Tornincasa, XP Power's industry director for the communications sector. In addition, "The power-factor-correction stage uses a silicon-carbide diode, which gives us almost a whole efficiency point," he says. The diode has lower noise and uses four to six fewer components than does a snubber circuit.

The supply is available in both a 12V version for intermediate-bus architectures and a 48V version for distributed-bus architectures, allowing you to use either isolated or nonisolated dc/dc converters. Units cost $82 (1000).

—by Margery Conner

▷**XP Power**, www.xppower.com.

The EMA212 achieves a power density of 10.55W/in.^{3} at an efficiency of 91% in a 1U form factor.

06.08.06

Audio IC controls power amp

Targeting audio-volume and -balance applications, the MAX5440 audio controller integrates a debounced rotary-encoder interface, wiper buffers, and two 40-kΩ-resistor strings. The interface uses gray-scale coding to move the wiper along the resistor string. The design eliminates the need for an external microcontroller, general-purpose IO chips, or bias circuitry. It connects directly to the output of the power amplifier. The controller operates from a 2.7V supply and uses less than 0.5 μA in standby mode. The IC sells for $1.47 (1000).

—by Maury Wright

▶**Maxim**, www.maxim-ic.com.

This audio controller eliminates the need for external microcontroller and I/O devices and offers volume and balance control.

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ANALOG DEVICES

Tool analyzes leakage for MTCMOS designs

Apache Design Solutions has released a new version of its Red Hawk power-analysis tool targeting leakage management. Transistor leakage became a problem at the 130-nm node when fabs began using thinner oxide transistors to improve design performance. Leakage got worse at the 90-nm node, and, at the 65-nm mode, leakage, rather than active power when a device is running, uses more than half of an IC's total power budget. According to Andrew Yang, Apache's president and chief executive officer, the tool addresses designers' need for a more aggressive leakage-reduction technique. He says that the semiconductor industry is reaching the limits of CMOS scaling, causing a power-versus-performance or leakage-versus-timing dilemma.

> "To keep improving performance, we need to keep drain-to-drain voltage high or keep the voltage threshold low.

"To keep improving performance, we need to keep drain-to-drain voltage high or keep the voltage threshold low," Yang says. To address this problem, most designers use a variable-threshold-voltage library, using low-voltage cells for critical paths and high-voltage cells for noncritical paths. "That technique can work in many applications to reduce power, but it doesn't work well for mobile-system applications that often employ a sleep mode," he says.

To reduce active power, designers often use active gating: reducing the number of switches in a design and thus power that switching consumes. However, to reduce leakage, designers employ power gating, in which they shut off the current to portions of the design. The MTCMOS (multithreshold-CMOS) power-gating technique, which TSMC (www.tsmc.com) employs, allows users to turn off the power to a given portion of a design using header and footer switches in NMOS and PMOS transistors, respectively. But using these switches increases area, and the switching creates additional power-supply noise that can interfere with the device's performance.

Designers use MTCMOS on the periphery of coarse-grained-architecture designs to power on and off voltage islands, whereas they employ MTCMOS throughout a fine-grained-architecture design's fabric. Coarse-grained architectures are more complex and have slower wake-up modes than fine-grained architectures, which offer greater power control but require more area and create more noise.

"This low-leakage-design technique does introduce additional design constraints to the power and noise nature of the design, so you need to carefully analyze it," says Yang. The Red Hawk LP (low-power) tool models a design's MTCMOS switches and all its logical instances and then performs dynamic transient analysis. This analysis supports mixed-design mode to account for blocks that are always on, blocks that are shutting down, and blocks that are waking up. The tool then analyzes the impact of the switches on timing and noise across the full chip.

The tool does full-chip analysis with transistor-level accuracy, says Yang. To get the tool to run a multimillion-gate design overnight and keep the transistor level accurate, Apache devised a nonlinear, large-signal-modeling technique. The tool gives power and performance results and calls out switch sizes and locations. Designers use the results of this analysis to optimize switch sizes and placement and refine their power-up and power-down strategies. The tool also analyzes structures unique to MTCMOS, such as instance-specific multivoltage cells, level shifters, and retention flip-flops. Red Hawk LP costs $275,000 for a one-year subscription.

—by Michael Santarini

▷**Apache Design Solutions**, www.apache-da.com.

06.08.06

Servo driver extends embedded platform

Targeting consumer electronics, industrial control, and automotive applications, National Instruments recently introduced a high-speed H-bridge servo-drive module for the CompactRIO embedded platform. The new NI 9505 drive module offers direct connectivity to actuators, such as brushed-dc servo motors, relays, lamps, solenoids, and valves.

Using CompactRIO's built-in FPGA and the LabView graphical-system-design software, designers can create intelligent, energy-efficient, and reconfigurable motion-control applications. By customizing FPGA logic, engineers can accurately control torque, velocity, and position and can implement advanced control techniques, such as the use of notch filters and gain scheduling. With the CompactRIO real-time embedded processor, they can implement functions such as supervisory control and trajectory generation for multiaxis coordination and accurate velocity and acceleration profiles for smooth movements. The NI 9505 delivers continuous current of as much as 8A at 40°C with a peak current of 12A at 30V, and it achieves 98% power efficiency. Prices for the NI 9505 start at $399.

The new NI 9505 H-bridge servo-drive module, along with graphical-design software, extends National Instruments' FPGA-based CompactRIO system into motion control.

—by Warren Webb

▶**National Instruments**, www.ni.com/compactrio.

DFM-tool start-up claims big power and yield gains

EDA-DFM (design-for-manufacturing) start-up BlazeDFM has announced its first tool, which it claims will reduce leakage power by as much as 40%, reduce leakage variability by as much as 60%, and improve timing by as much as 10% without the need for changing the layouts of 90- and 65-nm IC designs.

Chairman and Chief Technology Officer Andrew Kahng, a University of California—San Diego professor, started the company, along with one of his grad students, Product Architect Puneet Gupta. The third co-founder, Vice President of Marketing Dave Reed, is an EDA-industry veteran. The company also brought on former Forte Design Automation Chief Executive Officer Jacob Jacobbson to serve in the same post at BlazeDFM.

Reed says that more than 20 companies claim to be in the DFM market. However, BlazeDFM concentrates on only a subset of that market: electrical DFM. "DFM understands the things designers care about: power, performance, parametric yield, and cost," says Reed. He claims that other companies have only obliquely addressed these topics. "When you look at the parametric-yield issues, as BlazeDFM does," he says, "you can reduce by six months to a year the time it takes to get into volume production at acceptable yields, and you can reduce leakage power by 20 to 30%."

The company's tool, Blaze MO, runs concurrently with physical-verification tools. Users input GDSII (Graphic Design System II) and industry-standard formats. These formats include Verilog, LEF/DEF (library-exchange-format/data-exchange-format), DSPF/SPEF (detailed-standard-parasitic-format/standard-parasitic-exchange-format), .lib, and SDC (Synopsys Design Constraints) files. Blaze MO analyzes the layout and gate-length variability, or "slack," within the rules of a given foundry and creates an annotation layer in the GDSII to direct commercial OPC (optical-proximity-correction) tools to make adjustments to the design. "We put our annotations in a layer in the GDSII file, and, when it gets into manufacturing, the RET (reticle-enhancement-technology) tools can use those annotations to direct reticle enhancement," says Reed.

OPC tools cannot directly read the annotations, so OPC engineers must manually input them into the OPC tool of choice. Blaze MO has run silicon with both Mentor Graphics (www.mentor.com) and Synopsys (www.synopsys.com) OPC tools with similar results. OPC tools typically adjust layouts to ensure that each feature has the right size and shape and thus prints well in manufacturing. "Blaze tells what targets to hit on a transistor-by-transistor basis within the allowed processor range," Reed says. Blaze MO doesn't swap out custom cells for standard cells. Instead, the subtly altered shapes on a design have a profound impact on the design.

"To have a viable DFM offering, you need to offer value to both design and manufacturing," says Reed. "Blaze MO can help foundries make the same process look better to their customers without adjusting the equipment. It is possible to offer a half-node to customers—a process that is less leaky than, say, a foundry's standard 90-nm process."

—by Michael Santarini

▷**BlazeDFM**, www.blaze-dfm.com.

Pulse/pattern generators produce clean waveforms, clean user interface

Keithley Instruments' Series 3400 pulse/pattern generators provide high signal fidelity and precise control of pulse widths of 3 nsec to 1000 sec, as well as a simple, intuitive user interface. The generators suit use in semiconductor-device and material research in R&D and technology-development labs and in characterization and process integration in production and quality assurance. Pattern generation lets users simulate serial data to devices under test and determine the devices' performance characteristics in less-than-ideal situations. Applications include serial, wireless, and fiber-optic communication and nanotechnology-device development.

The product family comprises the $12,500, single-channel, 0.001-Hz to 165-MHz Model 3401 pulse/pattern generator and the $17,500, dual-channel, 0.001-Hz to 165-MHz Model 3402 pulse/pattern generator. Depending on the selected output impedance and external load resistance, the units produce signals as large as ±20V with little voltage overshoot, high amplitude accuracy, excellent flatness, and low edge-to-edge jitter. For remote control, the units include USB and IEEE 488 interfaces.

—by Dan Strassberg

▷**Keithley Instruments Inc**, www.keithley.com.

The Series 3400 pulse/pattern generators produce clean waveforms to 165 MHz and present users with a clean interface.

VOICES

Kris Pister and Ben Cook

Back to basics

Not too long ago, hotshot hardware-design engineers accrued bragging rights based on how many millions of transistors their chips had or how fast they were. Thanks to Moore's Law, transistors and speed are now less frequently the limiting factors of chip design. Rather, minimizing power and its attendant heat now indicates a clever design. And few applications face as many power constraints as the RF nodes in wireless-sensor networks, which are resilient, self-healing, and able to operate for years with no maintenance on standard AAA or coin-cell batteries.

As a professor of electrical engineering at the University of California—Berkeley, Kris Pister, also chief technical officer of wireless-sensor start-up Dust Networks, directs research into both the hardware and the software that these networks need. We talked with Pister and his graduate student Ben Cook about their research into ultralow-power radio design, which Cook recently presented at the International Solid-State Circuits Conference (**Reference 1**).

What was Cook's challenge?

A **Pister:** I told him to ignore all the conventional wisdom in radio design and trade off almost anything on the performance side to get to low power. He didn't end up trading much in the way of performance and still achieved low power: His radio burns 300 μW in receiving mode at 2.4 GHz, whereas the best commercial chips we're using right now at Dust Networks burn 30 mW. There's nothing in his radio that you can point to as radically lowering power consumption, but, if you look in CMOS-RF textbooks, all the basic ideas he used are there. It's just that most current radios have discarded them. Everything focuses instead on high performance at the expense of power.

Can you give three design ideas that really made a difference in power consumption?

A **Cook:** First, use a simple modulation scheme. For our applications, an extremely high data rate is unnecessary, so we can use BFSK [binary frequency-shift keying]. Plus, we added more frequency separation than is common. For example, Bluetooth also uses a form of BFSK, which has a data rate of, say, 1 Mbps, but it jumps between frequencies of only 320 kHz, and, as a result, it's a lot harder to demodulate than 1 Mbit with a frequency separation of a couple of megahertz.

Kris Pister has some things to say about ultralow-power radio design.

Second, passive-voltage gain is important. This idea flies in the face of current conventional wisdom that you've got to get your power gain at the beginning of the received-signal chain. CMOS devices take voltage, rather than power, as an input, and they have an almost purely capacitive input, so they can't absorb any power. If you apply your signal to the gate of a CMOS transistor, voltage amplification and getting that voltage gain using passive components that consume zero are the most important factors in overcoming the noise of that device.

A **Pister:** A subthread running through the design process was the additional goal of using as few off-chip components as possible. You hear a lot of people talking about single-chip radios, but that idea usually means a single silicon chip with all the transistors on it and then a bunch of passive components—crystals, filters, inductors, and other components—off the chip. He was shooting for not just the lowest power, but also the lowest cost in the smallest form factor in these radios, with a single chip with the absolute minimum number of components.

A **Cook:** Passive-voltage gain is not a universal solution. Some systems need power gain. For instance, cell phones have to interface to up-chip parts, such as SAW [surface-acoustic-wave] filters, and they need power gain in their amplifying stages, but we keep everything on-chip, and, therefore, we can interface to high impedances on the chip. So, we're not fixed to 50Ω, which RF components have traditionally used. We have flexibility with using voltage gain instead of power.

Third, minimize the overhead power consumption. For almost all radio topologies, you use a VCO [voltage-controlled oscillator] as the core of the transceiver, and we wanted to make it as low-power as possible, as well as eliminating as many other high-power blocks as possible. So, in the receiver, there's no RF amplifier in the front end, which is kind of a novel thing. Instead, the front end is a passive-voltage-amplifying network that goes straight to a passive mixer. Making everything passive in the front end drastically reduced power and still yielded good performance.

—by Margery Conner

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1 Cook, Ben, Axel Berny, Al Molnar, Steven Lanzisera, and Kris Pister, "An Ultra-Low-Power 2.4GHz RF Transceiver for Wireless Sensor Networks in 130nm CMOS with 400mV Supply and an Integrated Passive RX Front-end," IEEE International Solid-State Circuits Conference, February 2006, www.el.gunma-u.ac.jp/analog/ISSCC2006.pdf.

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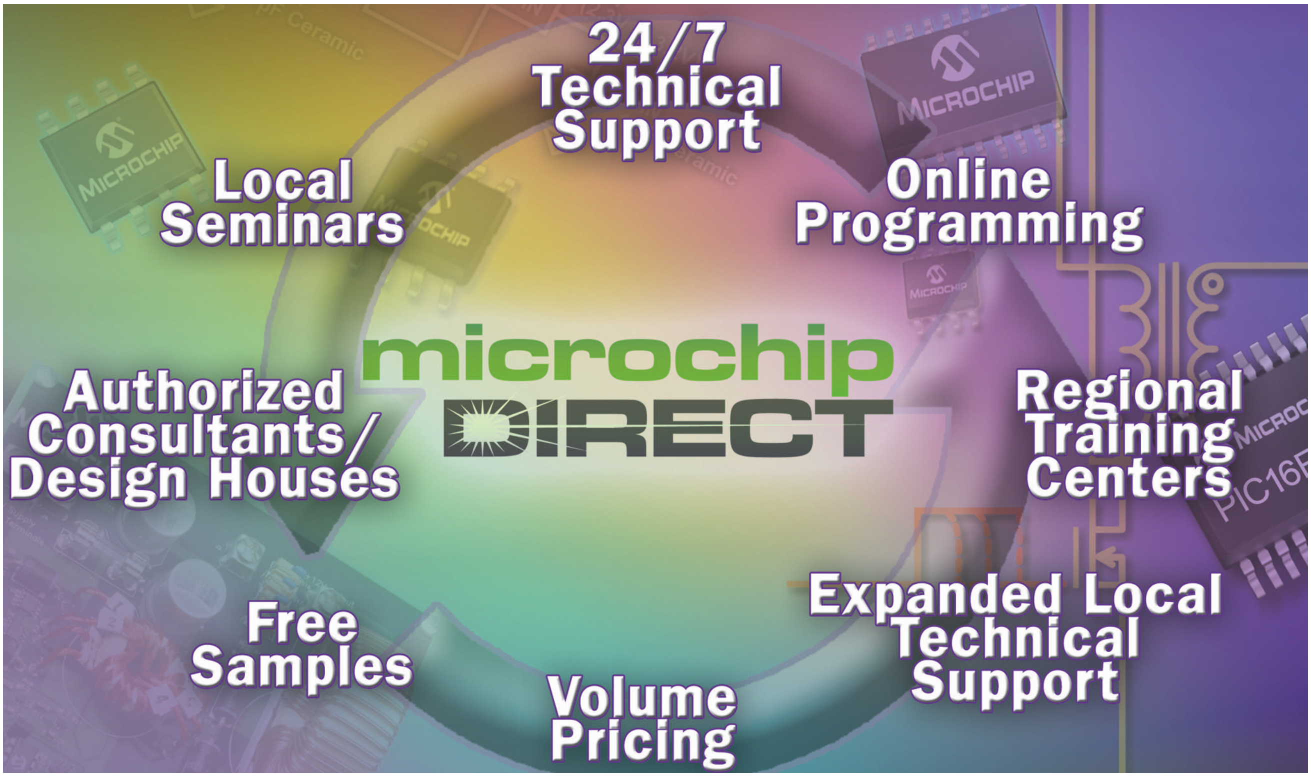

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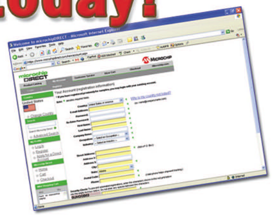

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GLOBAL DESIGNER

Module simplifies data acquisition with USB

National Instruments has introduced a data-acquisition system based on the connectivity of USB. The basic Compact DAQ hardware unit's eight-slot chassis accepts a range of hot-swappable, autodetected instrumentation modules. Although the unit does not replace the company's PCI-based instrumentation, NI says that, by exploiting the speed and convenience of USB 2.0, it can address the performance needs of a large fraction of the data-acquisition market.

Compact DAQ, the company says, operates equally well as a small-scale to midscale, quickly configured field-data-collection system, or as a small-scale ATE (automatic-test-equipment) platform. Modules provide signal conditioning for variables such as voltage, temperature, strain, sound level, and vibration. The system employs four dedicated USB-signal streams to provide the bandwidth to support as many as 256 measurement channels. You can combine low- and high-speed modules in the same configuration. According to NI, the diversity of currently available, capable ADC chips permits the company to build a variety of digitally isolated modules using ADCs. Compact DAQ operates from ac supplies or from 11 to 30V dc.

The basic Compact DAQ hardware unit's eight-slot chassis accepts a range of hot-swappable, autodetected instrumentation modules.

The LabView graphical programming environment supports the system through an open application-programming interface; you can also program it with Visual Basic 6 or with Microsoft Visual Studio .NET. Alternatively, you can use the DAQ Assistant, a set-up utility that offers a step-by-step configuration process that generates LabView code. Compact DAQ provides resolution as high as 24 bits and an acquisition rate as great as 3.2M samples/sec. You connect the eight-module chassis directly to a PC with a USB cable; connection requires no interface card. The speed of USB 2.0, NI points out, provides a channel into the PC that is almost five times faster than a 100-BaseT Ethernet connection, supporting fast data streaming. The unit's low latency enables fast command transmission. A base system of host frame and a four-channel, 10V-range measurement module costs about €1100 (approximately $1400).

—by Graham Prophet

▷**National Instruments**, www.ni.com.

Code verifies AHB designs

Advanced verification specialist EVE has selected silicon- and product-design-services company eInfochips to expand and complement the internally developed synthesizable transactor library for EVE's ZeBu emulation platform. The AMBA-AHB (Advanced Microprocessor Bus Architecture/Advanced High-performance Bus) transactor for EVE's ZeBu-UF/XL ASIC emulators complies with the AMBA-AHB 2.0 protocol. Users can employ it to verify AHB-slave designs on the ZeBu platform. "Our partnership with EVE will enable eInfochips to extend its functional-verification expertise to hardware-accelerator-based verification," says Tapan Joshi, vice president of marketing at eInfochips. "We look forward to developing a library of transactor IP [intellectual property] for various domains jointly with EVE and using this expertise to provide verification and validation services to our customers, ensuring successful tape-out."

EVE has previously announced that it will offer a catalog of peripheral-IP components to address the wireless; graphics, video, and multimedia; networking; and embedded-processor markets. These components—synthesizable memory models, hardware bridges, and synthesizable transactors—work with ZeBu. Transactors interface with a testbench written in C/C++, SystemC, or SystemVerilog at a high level of abstraction to a design under test mapped in ZeBu and mimic a specific protocol. EVE based the high-speed components on the ZeBu application-programming interface and will map them onto the RTB (reconfigurable testbench), EVE's proprietary and patented technology.

—by Chitra Giridhar, *EDN Asia*

▷**EVE**, www.eve-team.com.

▷**eInfochips,** www.einfochips.com.

Microcontroller hits nanoamp-current levels

06.08.06

Four 8-bit AVR-architecture picoPower microcontrollers from Atmel have current demands of 300 μA when active; 150 μA in idle mode with a 1-MHz clock; 650 nA in power-saving mode, which operates a 32-kHz clock and a brownout-watchdog circuit; and 100-nA in full power-down mode. Atmel designed this variant of the AVR family for use in battery-powered systems in which the processor has a low duty cycle, spending most of its time in sleep mode. Examples include lighting control; security; keyless entry; wireless protocols, such as ZigBee; and other low-data-rate applications.

Atmel says the power savings come from concentrating design effort on reducing crystal-oscillator power consumption, brownout detectors (a requirement to identify a failing battery in a long-life application), and I/O-pin leakage. The parts are pin-compatible with other AVR-architecture devices.—by Graham Prophet

▶**Atmel**, www.atmel.com.

Microsoft

Real-time monitoring for critical patient care. That's the Power of Windows Embedded.

Getting real-time patient monitoring devices into the hands of doctors and nurses can save lives. That's why the engineers at Zoe Medical chose the speed and reliability of Windows CE to develop their Nightingale Personal Patient Monitor (PPM2) and make it available to hospitals in just 12 months.

With only two developers and a short timeframe, Zoe Medical took advantage of the shared source code in Windows CE to move its applications from its traditional MS-DOS platform to a system that is more flexible, familiar, and provides the graphic and audio support its customers demand. Plus, the hard real-time performance of Windows CE met the strict requirements of the PPM2 to monitor and communicate vital patient functions as they happen.

"We took two critical patient care devices to market in only a year. Windows CE was a big part of that achievement."

—JIM CHICKERING/Clinical Applications Manager
Zoe Medical Development

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Windows Embedded

BY BONNIE BAKER

Choosing antialiasing-filter amplifiers

When you digitize an analog signal, you use a lowpass filter to prevent aliasing errors from out-of-band noise. Doing so attenuates superimposed, high-frequency noise on the analog signal before it reaches the ADC. If the noise on the input signal is more than half the sampling frequency of the converter, the magnitude of that noise stays the same, but the frequency changes as it aliases back onto your signal of interest. You cannot use a digital filter to reduce in-band noise after digitizing the signal.

Selecting the correct operational amplifier for an active lowpass-filter circuit can appear overwhelming as you read an amplifier's data sheet and view all of the specifications.

Before selecting the amplifier, however, you need to determine the filter-cutoff frequency, f_{CUT} (or −3-dB frequency). You can use filter-design programs to determine the filter's capacitor and resistor values.

Next, you should initially consider only two important specifications when selecting an amplifier for your active lowpass filter: gain-bandwidth product and slew rate. In **Figure 1**, for Q_i of less than 1, the gain-bandwidth product of the amplifier, f_{AMP}, must be at least $100\times gain\times f_{CUT}\times k_i$, where Q_i is the quality factor of the i^{th} partial filter and k_i is the ratio of the partial-filter-corner frequency to the overall-filter-corner frequency. For Q_i greater than 1, $f_{AMP}=100\times gain\times(f_{CUT}/a_i)\times\sqrt{[(Q_i^2-0.5)/(Q_i^2-0.25)]}$, where a_i is the i^{th} coefficient in the partial-filter-transfer function. The gain-bandwidth product of the operational amplifiers appears in the specification table of the respective product-data sheet.

You should also evaluate the effects of amplifier slew rate. Doing so ensures that your filter does not create signal distortions due to slew limitations. The slew rate depends on internal IC currents and capacitances. When you send large signals through the amplifier, internal currents charge these internal capacitors. The speed of this charging process depends on the amplifier's internal resistances, capacitances, and currents. To ensure that your active filter does not enter into a slew condition, you need to select an amplifier such that the slew rate$\geq(\pi V_{OUT\ P\text{-}P}f_{CUT})$, where $V_{OUT\ P\text{-}P}$ is the expected peak-to-peak output-voltage swing below your filter's cutoff frequency.

The most common topologies for active, second-order, lowpass filters are the noninverting Sallen-Key and the inverting multiple feedback (**Reference 1**). If you need a higher order filter, you can cascade both of these topologies (**Reference 2**).

When using the Sallen-Key circuit, input-common-mode-voltage range (V_{CMR}) and input bias current (I_B) can also affect you. In this configuration, V_{CMR} limits the range of your input signal. Additionally, the input bias current conducts through the external source resistance. The voltage drop that the input-bias-current error causes appears as an additional input-offset voltage. Also, be aware that this circuit has high-frequency feedthrough. EDN

A FEW BUTTERWORTH-DESIGN CONSTANTS

FILTER ORDER	i	a_i	$k_i=f_{CUT-i}/f_{CUT}$	Q_i
4	1	1.8478	0.719	0.54
	2	0.7654	1.390	1.31
5	1	1	1	NA
	2	1.6180	0.859	0.62
	3	0.6180	1.448	1.62

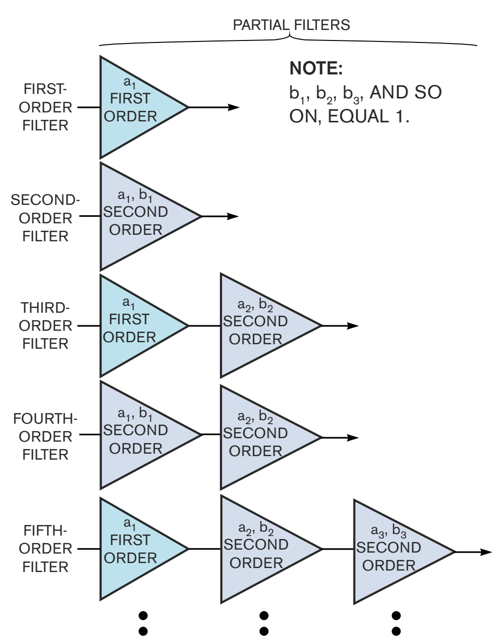

Figure 1 You build a multi-order analog filter by cascading first- and second-order filters.

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2. Mancini, Ron, *Op Amps for Everyone*, ISBN-0-7506-7701-5, Elsevier-Newnes, April 2003.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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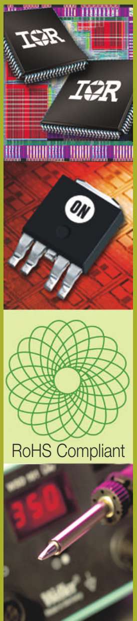

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Dropped call: breaking down a broken cell phone

"One man's trash is another man's treasure." That's the thought that ran through my mind when I discovered a Sanyo MM-8300 advanced cell phone, snapped into two pieces at the clamshell hinge and lying in the curb near my home office. What's under the phone's fashionable plastic skin, and how did Sanyo squeeze such a plethora of functions into a 3.35×1.85×0.97-in. (85×47×25-mm), 3.60-oz (102g) form factor?

PRY FURTHER AT EDN.COM

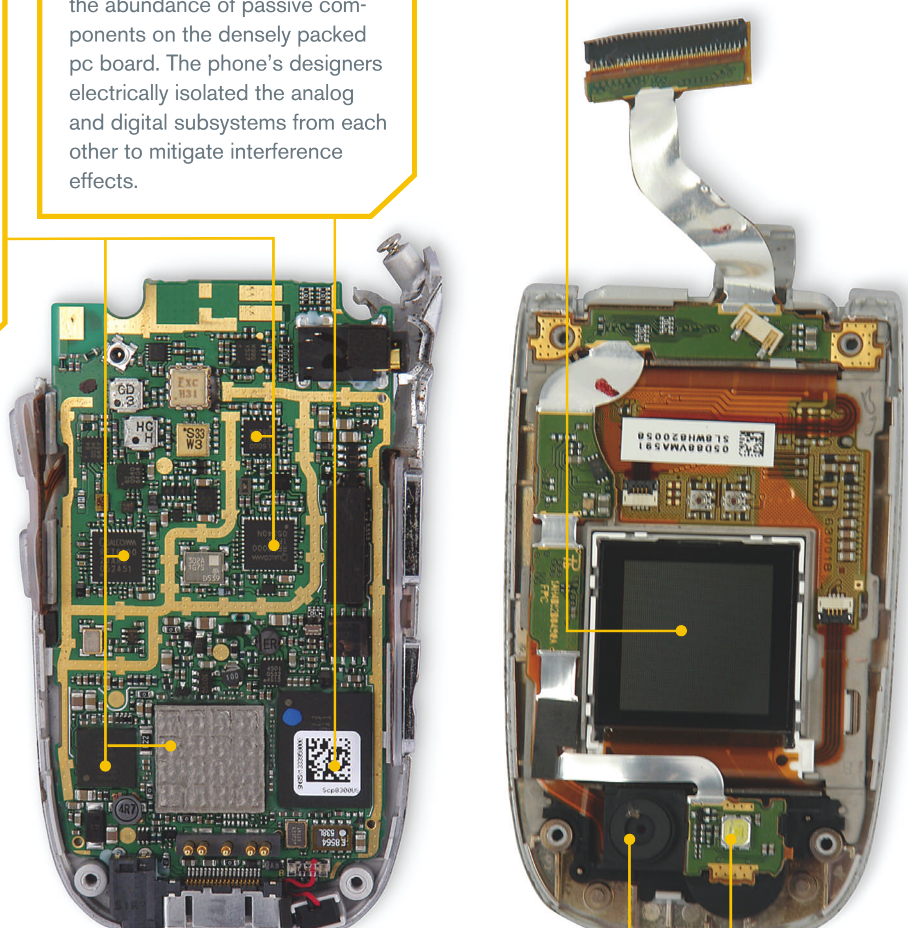
For expanded analysis and additional internal pictures of the MM-8300, visit www.edn.com/060608pry. You can also search the Federal Communications Commission's Web site (www.fcc.gov) for documentation, using approval ID number AEZSCP-83H.

The MM-8300 includes a 1.8-in.-diagonal, 176×220-pixel primary LCD and a 1-in., 72×72-pixel secondary LCD, each of which can resolve 64,000 colors. Cellular voice modes include 850-MHz AMPS (Advanced Mobile Phone System), both 850- and 1900-MHz CDMA (code-division-multiple-access), and Sprint's Ready Link "walkie-talkie." The MM-8300 also supports 1×RTT (radio-transmission-technology) cellular-data services, such as WAP (Wireless Application Protocol) 2.0-compatible browsing.

Another cryptically labeled chip is, I suspect, a single-chip, multi-die, stacked combination of RAM and flash memory under the ROM-code sticker. Notice, too, the abundance of passive components on the densely packed pc board. The phone's designers electrically isolated the analog and digital subsystems from each other to mitigate interference effects.

Qualcomm (www.qualcomm.com) chips form the silicon foundation of the phone's design: the MSM6100 application processor, which resides under a thermal pad; the RFL6000 low-noise amplifier; the RFR6000 RF-to-receiver-baseband converter; the RFT6100 transmitter-baseband-to-RF converter; and the PM66x0 power-management IC, if that is indeed what the cryptically labeled "BH6318GL" chip is.

The flash-inclusive embedded camera captures 640×480-pixel VGA-resolution still images, along with video streams as long as 30 seconds in 176×144- or 128×96-pixel resolution. Java 2 Micro Edition and 3-D-graphics capabilities provide numerous application opportunities; the MM-8300 also supports Sprint's streaming-audio and -video services.



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Rick Matz, Senior Applications Engineer,
Fujitsu Microelectronics America, Inc.

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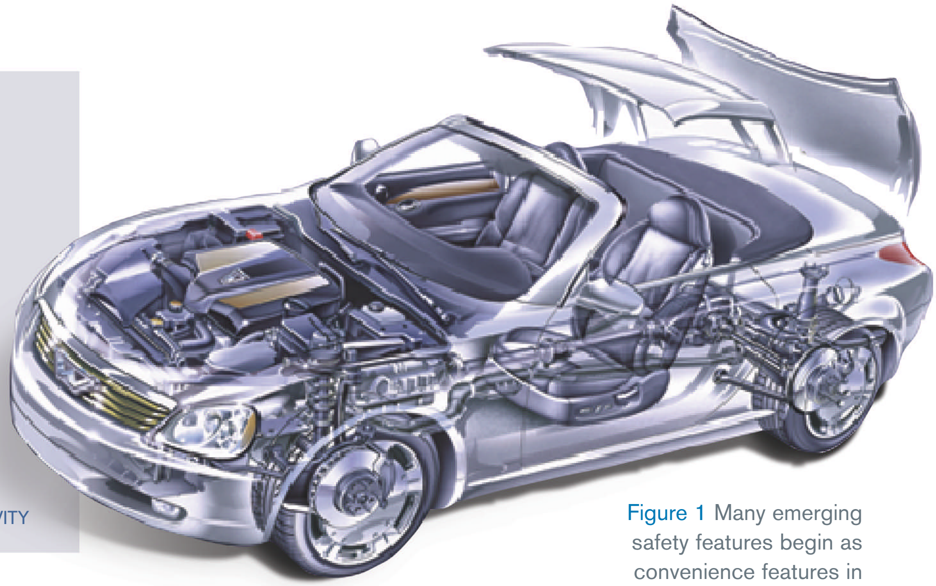


Figure 1 Many emerging safety features begin as convenience features in high-end vehicles. Contemporary middle-class cars contain around 30 electrical/electronical systems, 50 to 100 microprocessors, and more than 100 sensors (courtesy Robert Bosch GmbH).

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

MAKING VEHICLES SAFER BY MAKING THEM SMARTER

NEW FEATURES MUST BE SMARTER TO ADD VALUE WITHOUT DISTRACTING THE DRIVER AND INCREASING THE RISK OF ACCIDENTS.

According to semiconductor-market-research company IC Insights, electronic content made up 23% of the total price of an automobile in 2004, and it will make up 40% of the price by 2010. Many of the earliest in-car electronic systems replace mechanical systems, and they provide more efficient operation of the vehicle for lower cost and higher reliability than the mechanical systems they replace. More recent in-vehicle electronics manage safety systems, such as air bags and intelligent restraint systems, which automatically attempt to adjust and change the environment in the vehicle to minimize the risk of serious injury and death to drivers and passengers while a crash is occurring.

In addition to new safety features, automobiles are incorporating more convenience features for assisting the driver and for providing passengers with information and entertainment. Car manufacturers usually isolate the electronic systems for passengers from the convenience and safety systems that assist the driver. This article focuses on those electronics that are available or are in development that improve the driver's ability to direct and operate the vehicle.

An increasing number of emerging safety features, such as object detection around the vehicle, begin as convenience

AT A GLANCE

- Driver inattention is the leading factor in most accidents.
- Electronic systems offload some of the cognitive load from the driver.
- In-vehicle crash-avoidance features must accurately correlate a risk condition with the driver's intent.

features in high-end vehicles (**Figure 1**). The feature supports adaptive cruise control, in which the system enables the vehicle to adjust the cruising speed based on the road position; distance; and relative speed of objects, such as other vehicles, without explicit driver intervention. A different implementation of the feature enables parking assistance and blind-spot-warning systems that can alert the driver when there is an object or vehicle in a risky position relative to the driver's likely goal position.

COGNITIVE CYCLES

An explicitly acknowledged value of convenience and safety systems for drivers is that they can make driving safer, easier, or less stressful. The implied value of these systems is that they might be able to alert and direct a driver's attention to an important detail, thereby avoiding an accident. Peter Schulmeyer, director of strategy for Freescale's Transportation and Standard Products Group, points out, "A main aim of in-car electronic systems currently in development or early deployment is to reduce the load on the driver."

In 2004, police reported approximately 6.2 million motor-vehicle accidents that killed 42,636 people and injured approximately 2.8 million (**Reference 1**). According to an NHTSA (National Highway Traffic Safety Administration) report and the VTTI (Virginia Tech Transportation Institute), driver inattention is the leading factor in most crashes and near-crashes. The report found that 80% of collisions and 65% of near-collisions involved driver inattention, such as from drowsiness or cell-phone use, within three seconds before the event.

The development and deployment of passive safety systems, which improve a vehicle's crash worthiness and survivability, are experiencing diminishing returns on the effort to improve them. Examples of preconditioning systems include tightening the tension in seat

IN-VEHICLE NETWORKS

The LIN (local-interconnect-network) protocol enjoys widespread use in vehicles. It optimizes communication between user modules with low-speed transmission requirements to 20 kbps for applications such as seat, mirror, and power-window adjustments. Another in-vehicle communication protocol, MOST (media-oriented systems transfer), succeeds the D2B (Domestic Digital Bus) protocol, and it targets multimedia applications.

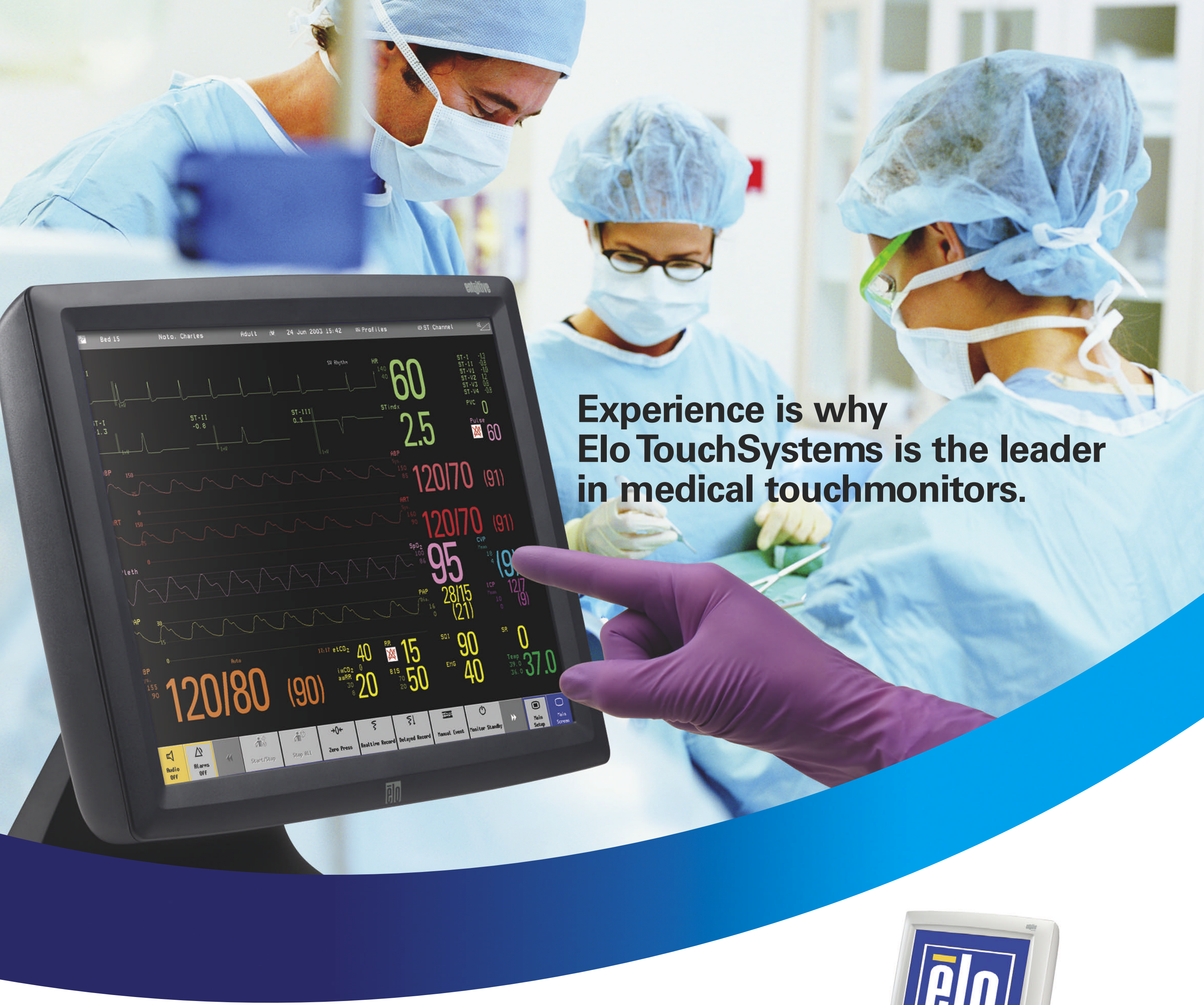
The CAN (controller-area-network) protocol has replaced many proprietary systems to link the various electronic subsystems, including the engine controller, power train, and emission controller, in a vehicle. CAN implementations support real-time communications with low-cost, off-the-shelf components in harsh environments. CAN employs CSMA/CR (carrier-sense multiple access with collision resolution), a nondestructive, bitwise-arbitration scheme. The CAN protocol enables maximum bus usage during a bus conflict by sending higher priority messages first. CAN's maximum achievable data rate is 1 Mbps, and the limiting factor on the maximum bus capacity is the response time. The maximum latency for the highest priority messages is approximately 150 msec. During the early stages of the design, the designer assigns a numerical value to a message, which establishes its priority; the message's identifier contains this value. The lower the numerical value, the higher its priority.

The FlexRay Consortium has since 2000 been developing the FlexRay communications technology, which targets high-speed control applications in vehicles to increase safety, reliability, and comfort. FlexRay is positioning itself as a substitute for CAN for those applications that require data rates beyond what CAN supports or having multiple CAN buses in parallel. FlexRay also suits automotive backbones to provide connectivity between several networks.

FlexRay supports two communication channels, each operating at a 10-Mbps data rate. The protocol uses an access method based on a synchronized timebase, and it organizes messages so that each has a known latency within a guaranteed tight variance. FlexRay can optionally redundantly transmit individual messages to provide an additional layer of network reliability and maintain the most efficient use of the network bandwidth.

FlexRay supports flexibility in optimizing the system for availability or for throughput by supporting static- or dynamic-bandwidth allocation, respectively; this approach allows designers to extend a system without adjusting the software in the nodes. FlexRay supports bus and star topologies and a variety of configuration parameters, such as the duration of the communication cycle or the message length.

Migrating from event-driven CAN to time-driven FlexRay communication is a paradigm shift for in-vehicle communication, and it requires retraining of all involved parties. For example, start-up is one of FlexRay's most complex operating phases because the communication is based on a fault-tolerant, synchronized clock scheme that has no master to set the timebase at start-up. Instead, you must use an alternative procedure to establish a timebase. The adoption of FlexRay will take some time.



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belts, moving the seats into a position best for the safest air-bag deployment, and closing the windows and sunroof in response to an imminent crash. The findings of this report support the significant value potential for electronic systems that can bridge the driver-inattention gap. This realization is pushing the focus of new systems for active roles that can alert the driver or actively affect how the vehicle is operating to avoid an accident in the first place (**Figure 2**).

As automobiles become more autonomous, the driver's focus will be able to shift toward directing the vehicle to the destination and away from the mechanics of operating the vehicle. Adaptive cruise control, for example, uses radar (radio detection and ranging) to maintain a safe distance from another vehicle while traveling on the road, thus offloading some of the cognitive load from the driver and filling in for the driver during moments of inattentiveness. The system can more quickly and more precisely respond than the driver to changes in speed of the leading vehicles.

Electronic stability control combines antilock brakes, traction control, and yaw control to assist the driver to maintain control of the vehicle. The system operates by comparing the direction the driver wants to go with the vehicle's actual response; it accomplishes this task by correlating the steering-wheel and braking sensors with sensors measuring vehicle yaw and roll acceleration, as well as the rotation of each wheel. When the system detects differences between the driver's commands and the vehicle's behavior, the system intervenes by applying braking forces to the appropriate wheels to correct the path of the vehicle for understeering and oversteering. The system may also include a connection to the vehicle's power-train controller to reduce the engine torque as needed.

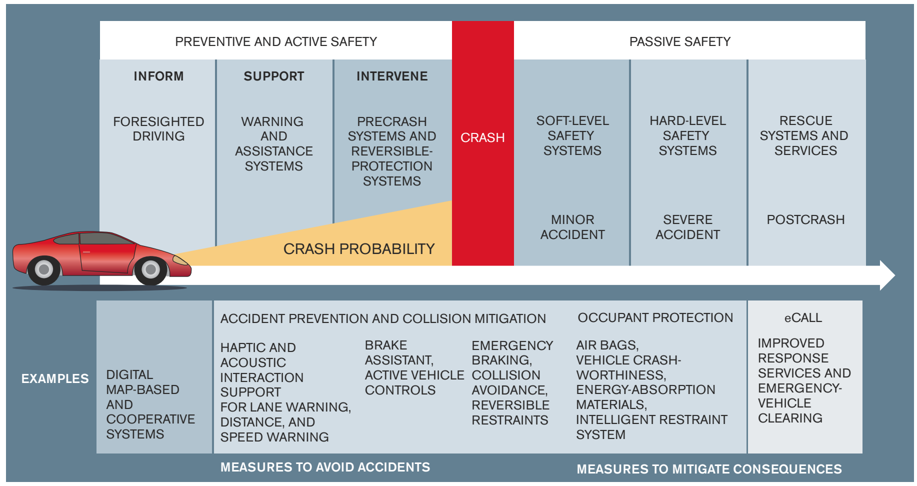

Figure 2 Depending on the significance and timing of a threat, the active and preventive safety systems inform the driver as early as possible, warn the driver if there is no driver reaction to the information, and actively assist or intervene to avoid an accident or mitigate its consequences (courtesy PreVent).

INFER INTENT

To provide capabilities that help avoid crashes, systems need to be able to recognize potential crash indicators seconds before an accident occurs. It is important for a safety system to be able to infer the driver's intent and correlate that intent with the vehicle's behavior so that the system can avoid taking predictive action based on false and incorrect conclusions. Active safety systems that intervene as a crash is beginning become active within a fairly narrowly defined set of conditions and are associated with the vehicle's acting in an unstable or a distressed manner.

For systems that predict and recognize potential threats with time to avoid the threat, the need to accurately infer the driver's intent is more important and difficult. First, false alarms immediately erode and quickly destroy the value of the warnings because the driver either turns off the system or ignores the warning. For these systems to be effective, they must alert few or no false or irrelevant conditions to the driver. For example, for a driver that follows a consistent sequence of starting the vehicle first and immediately putting on a seat belt, the seat-belt-warning system offers marginal value because it always alarms when the car is turned on.

The challenges facing a blind-spot-detection system illustrate the need to infer the driver's intent. If the system warns the driver whenever an object was in the blind spot, the driver would quickly disable the system. To be useful, the system should warn the driver of a blind-spot condition only when the driver intends to change the vehicle's position such that a collision with the detected object is a real possibility. This requirement complicates the task of notifying the driver of a blind-spot condition beyond just detecting the object. Examining a single driver control, such as the turn signal, is insufficient to accurately determine that the driver intends to change lanes.

In addition to the sensors detecting the environment outside the vehicle, the sensors to infer the driver's intent can include collecting inputs from multiple points, such as the steering wheel, the brake pedal, the turn signal, the vehicle's inertial and acceleration-measurement systems, and even examining the driver's body language through an in-cab vision system. No industry-standard algorithms exist for inferring the driver's intent to change lanes; such algorithms are the result of independent, proprietary research and development by the Tier 1 automotive suppliers.

SENSOR FUSION

To support the need for high accuracy when acting on a risk condition, these systems are receiving inputs from multiple sensors and types of sensors. Each type of sensor has strengths and weaknesses, and, by combining different types of sensors to cross-correlate redundant information, the systems can make better decisions. Manufacturers are deploying or exploring such technologies as radar, LIDAR (light detecting and ranging), infrared, ultrasonic, and video for perceiving the environment (**Figure 3**). Each of these sensor technologies overlaps with the others, but each one provides unique strengths in

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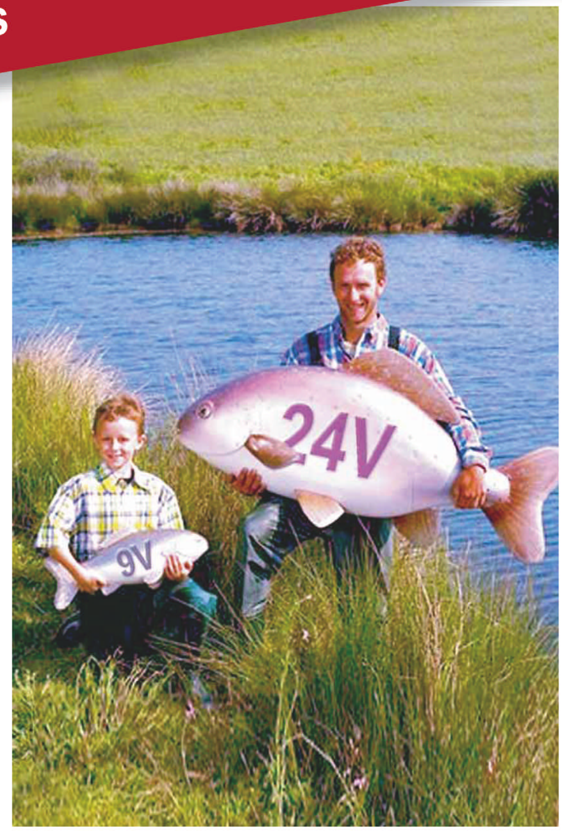

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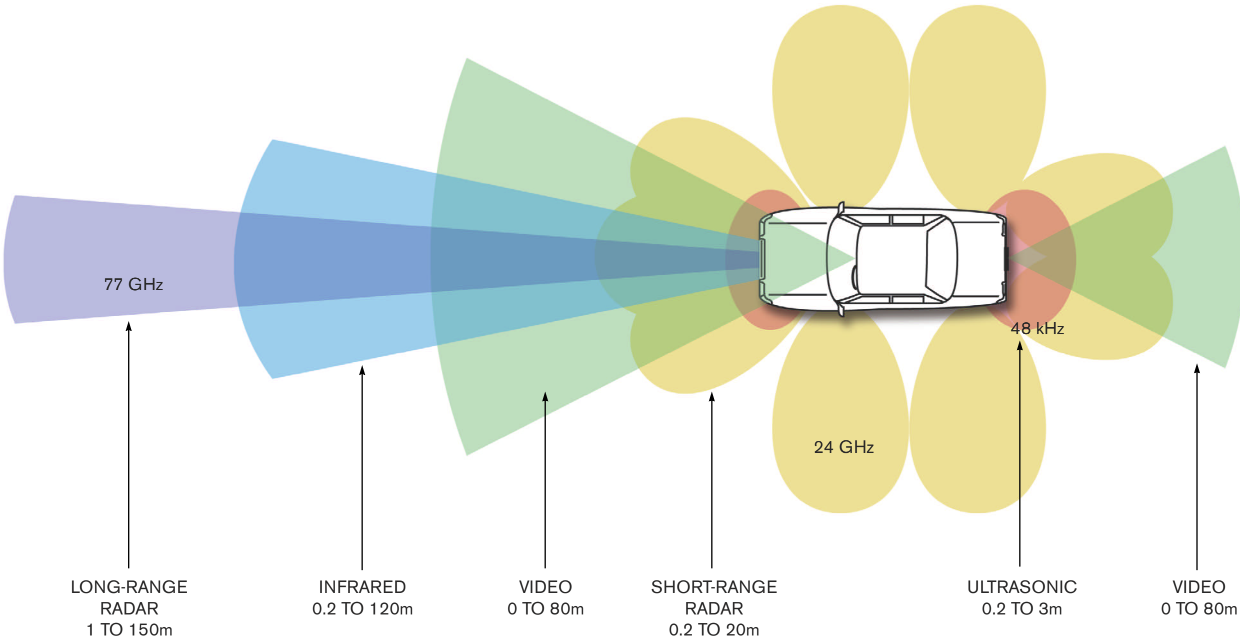

Figure 3 Sensor fusion, the combining and correlating of data from multiple types of sensors, allows vehicle systems to better identify and accurately recognize conditions inside and outside the vehicle (courtesy Robert Bosch GmbH).

different regions of the vehicle.

Some car makers are mounting cameras in and on vehicles. The cameras point not only outward from, but also inward to the vehicle. Outward-pointing cameras can complement the other outward-pointing sensors by providing details that enable the system to perform not just object detection, but also object recognition to support behavior prediction. Inward-pointing cameras provide the system with occupant information, such as size, position within the seat, body language, and even facial expressions. Inward-pointing cameras support functions such as smart air-bag deployment, as well as detect when the driver experiences drowsiness or intoxication.

The camera sensors continue to improve. For example, cameras that can support HDR (high dynamic range) can collect better image details across a wider range of lighting conditions than can cameras with a linear range. HDR-capable sensors are important for use with cars because they must operate in dark and bright environments. An HDR sensor, in contrast to a linear sensor, can detect details that bright environments wash out, and it misses fewer details in dark environments (**Figure 4**). HDR shines in situations in which both dark and light regions exist in the same scene. The linear mode of operation affords greater differentiation between brightness levels if the scene maintains one range of light level.

Other relevant sensor inputs capture information about the vehicle's behavior. These sensors include gyroscopes, accelerometers, steering-wheel- and brake-pedal-position detectors, and tire-rotation-rate systems. Another source of information includes in-vehicle knowledge of what the environment should contain through the use of digital maps with positioning systems such as GPS (global positioning system). Devices embedded in the road can wirelessly provide additional local and real-time information to the vehicle.

"Data fusion" involves combining these sensors and correlating their inputs. These inputs can enable the vehicle's electronic systems to identify its position and path relative to other objects near the vehicle, but, as these systems collect data from more types of sensors, there is an increase in the amount of needed real-time processing performance and of data that must traverse the in-vehicle networks (see **sidebar** "In-vehicle networks").

The vehicle network not only decreases the cost and weight of the vehicle by reducing components, but also enables designers to reduce or eliminate redundant sensors. For example, the air-bag and chassis system can share a gyro to sense the vehicle's stability and a rollover or impact condition. Sensor or data fusion may even enable designers to eliminate sensors or measure variables that are difficult to place a sensor near with virtual sensors. Possible opportunities for virtual sensors include measuring tire pressure and road-surface type and friction.

HUMAN-MACHINE INTERFACE

The biggest challenge for electronic assist, convenience, and safety features may be in implementing the HMI (human-machine interface). The HMI must ensure that each of the predictive, active, and preventive systems in the

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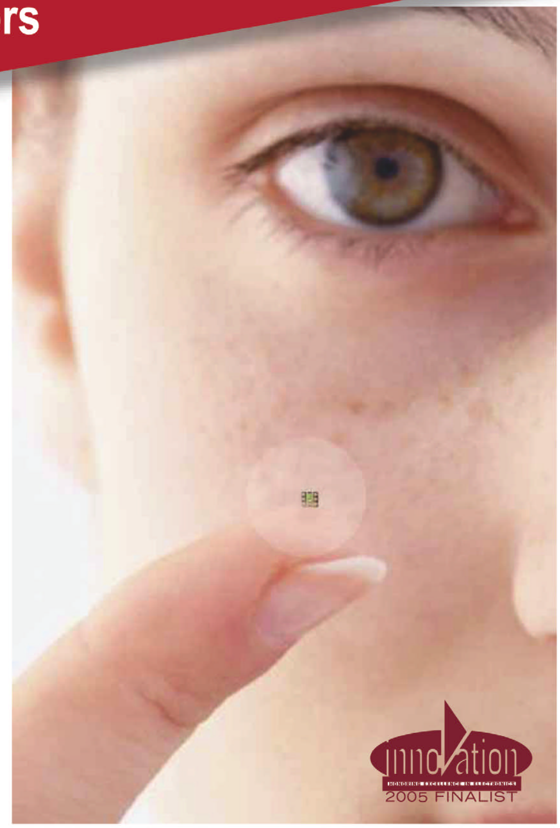

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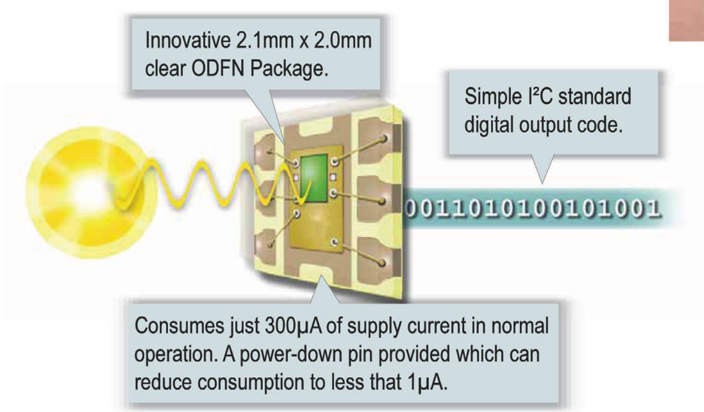

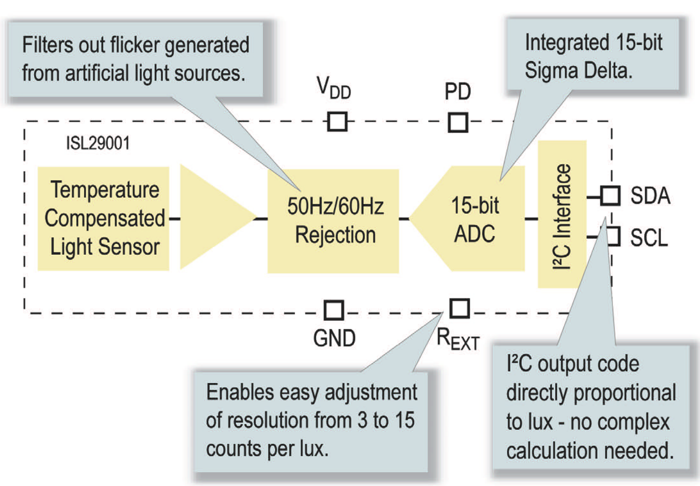

ISL29001 Key Features:

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vehicle operates according to the expectations and the ergonomic and cognitive limitations of the driver. These features support the driver, and that support can have unintended consequences in how the driver's behavior may change in different situations.

As these systems become more autonomous, the driver has less control of the vehicle. Systems that are partially autonomous may make driving more dangerous because they may contribute to more inattentiveness from the driver; the driver's response time could suffer in those events that require a decision. For example, if a collision is likely, which of two vehicles should the car hit to avoid hitting the other? What if the choice is between two pedestrians? Manufacturers cannot leave all of the decisions to the vehicle's control system until it can accurately recognize these concepts and make appropriate decisions based on other external factors at the time of the incident.

The HMI must consider the cognitive load on the driver. The way it presents data to the driver is an important consideration. The idea of presenting everything to the driver on a display is a tempting idea, except that using a display demands the driver's attention and constant polling to interpret the presented data. The display could become a distraction from the road because the cognitive burden may be too much if the display is the mechanism to deliver warnings while driving. The more information available on the display while driving demands the driver to perform more cognitive processing to filter and interpret the data.

Telematic systems can offer a lot of convenience and value to a driver, but how the driver interacts with these systems is important. Merely switching radio stations proves to be a significant cognitive burden or distraction to a driver's maintaining attention on the road. VoiceBox's Telematics Navigator is an

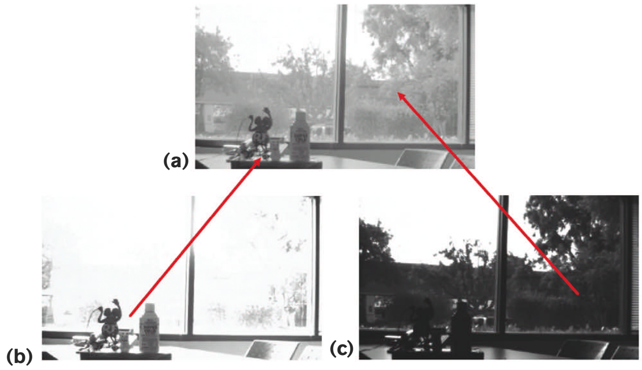

Figure 4 Improvements in sensors include the ability to collect better data over a wider range of conditions. The HDR (high-dynamic-range) ability of a camera system (a) enables the camera to see better details than a linear mode allows in an environment with extreme dark (b) or bright (c) lighting (courtesy Kodak).

approach to reducing the cognitive load on a driver to navigate radio stations, as well as other telematic services that will become available to drivers. The system promises to allow the driver to use conversational language to search and navigate capabilities. Check out the "VoiceBox and XM" link in the "More at EDN.com" box for a four-minute video demonstrating the system.

As the cost of the underlying components for these types of systems continues to decrease, the opportunities for new in-vehicle-electronics convenience and safety features will increase. Moving in lock step with the decrease in component prices is the building of the software layers for precursor functions that support more complex functions with more intelligence. Enabling software reusability and verifying increasingly complex systems at an industry level are keys to the forward momentum of these systems. AUTOSAR (Automotive Open System Architecture) is attempting to address the basic infrastructure for the management of functions for future applications and software modules.

One last hurdle for these emerging systems is the cultural acceptance of letting the automobile take over more of the tasks of driving. A complaint from driving enthusiasts about the existing systems, such as electronic stability control, is that they make driving less fun. Also, as these systems become more interdependent, the opportunity for self-adjusting the vehicle will decrease as such changes could adversely affect the performance of the entire system. The underlying concept of these types of systems is appropriate for any type of vehicle, such as planes, trains, and boats—not just automobiles. The success of one system in one type of vehicle could translate to acceptance in another type of vehicle. EDN

MORE AT EDN.COM

⊞ For more from Robert on autonomous systems, read www.edn.com/article/CA6288032.

⊞ Robert takes a look at telematics at www.edn.com/article/CA336885.

⊞ Go to the "VoiceBox and XM" link at the Web version of this article at www.edn.com/060608df1. While there, you can click on Feedback Loop to post a comment on this article.

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You can reach Technical Editor Robert Cravotta at 1-661-296-5096 and rcravotta@edn.com.

FPGAs BALANCE LOWER POWER, SMALLER NODES
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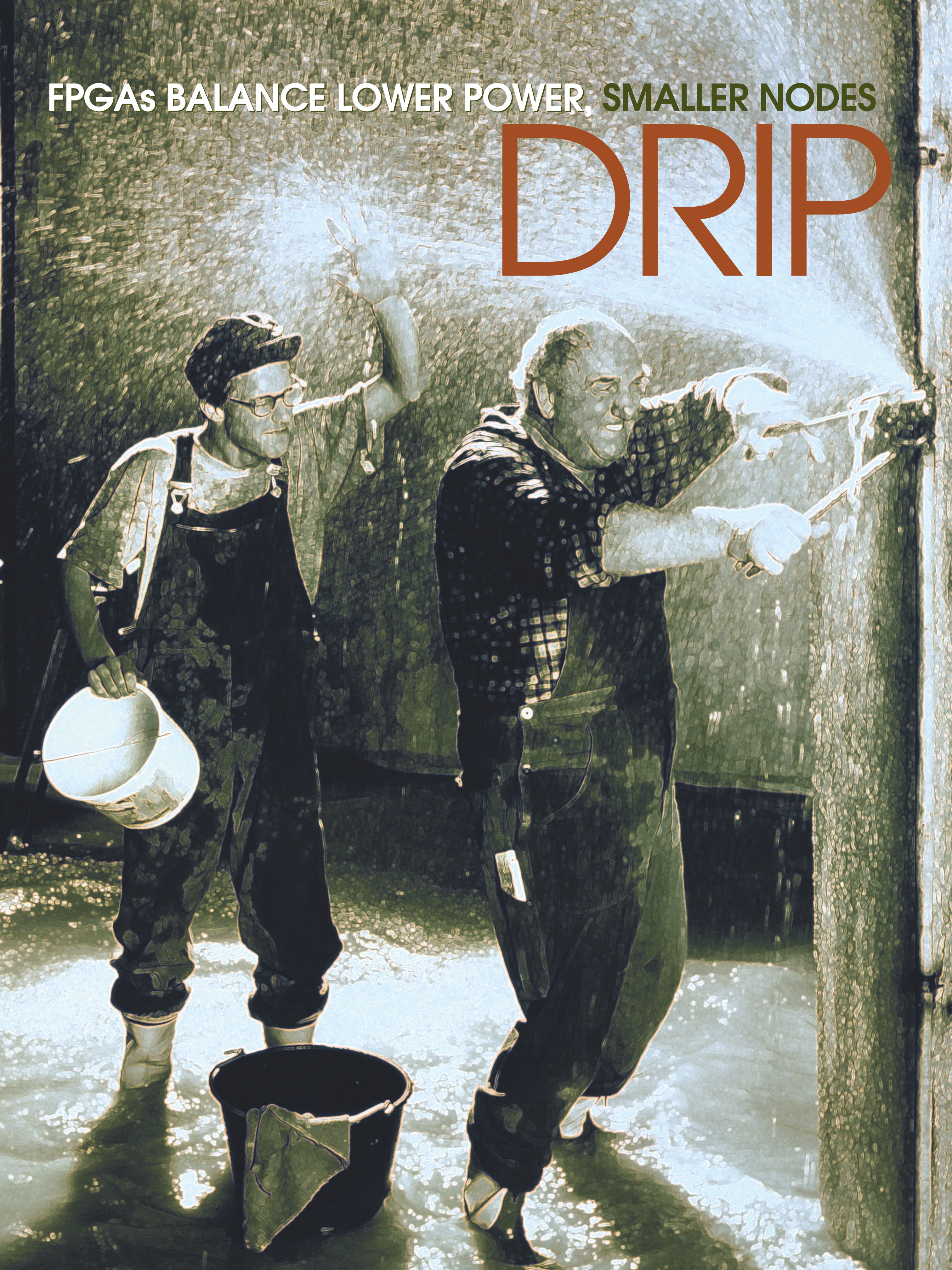

BY MICHAEL SANTARINI • SENIOR EDITOR

BY DRIP

THE FPGA INDUSTRY FACES THE SISYPHEAN TASK OF ADDRESSING DEMAND FOR LOW-POWER OPERATION, EVEN AS VENDORS FACE THE LURE OF PERFORMANCE, DENSITY, AND PRICE-PER-GATE ADVANTAGES OF THE 65-NM-PROCESS NODE.

ABOUT EIGHT YEARS AGO, just when FPGA vendors figured out how to increase the gate counts of their devices to rival those of ASICs, the market started demanding higher performance. It took the industry about four years to make these now-million-gate devices run at speeds comparable with those of ASICs. But it did so just as the market made low-power devices its top priorities. So, once again, the FPGA vendors are trying to address demand for low-power operation as they approach ever-smaller process nodes.

This time, however, the task of meeting market demand is more challenging because, in making FPGAs larger and faster over the years, FPGA-chip architects squeezed more power and capacity from silicon mainly at the expense of increasing power consumption. FPGAs got most of their speed increase over the years from using thin-oxide transistors that grow thinner with every process reduction. Thinner gate oxides come with a nasty side effect: They leak power, and leakage, or static power, produces heat. Starting at the 130-nm node, static power in transistors began to explode. It got worse at 90 nm, and, if manufacturers fail to address the issue, it would get exponentially worse at 65 nm (**Reference 1**).

In the race to have the fastest, highest capacity parts in the 65-nm node, Xilinx and Altera have made power management a top priority. Neither has produced a low-power miracle, so it's unlikely that large FPGAs are going to give ASICs a run for their money as the primary chips in large-quantity consumer-handheld-electronics applications, such as cell phones (see **sidebar** "What drives FPGAs' demand for low power?"). FPGAs still consume 400 times more power than their ASIC equivalents. However, FPGA vendors have seemingly made admirable progress toward stopping the leakage at the 65-nm-process node and make devices at those nodes less power-hungry than their 90-nm devices.

Xilinx claims that it has stabilized leakage and reduced dynamic power from 10 to 50%, depending on configuration, so that its 65-nm Virtex-5, which the company released in May, has an overall lower power consumption than its 90-nm V4 device but with 65% greater density, 30% better performance, and 45% less die area. Meanwhile, Altera claims that users will be able to configure its upcoming 65-nm Stratix III device, due out next year, to consume on average half the power of its 90-nm Stratix. Further, it claims that the 65-nm family will be the highest per-

AT A GLANCE

- FPGAs are 400 times more leakage-prone than their ASIC equivalents.
- Xilinx and Altera are stabilizing leakage in their 65-nm devices to the level of their 90-nm devices.
- Xilinx's and Altera's 65-nm devices will have lower dynamic power than their 90-nm devices.
- The companies achieve most of their dynamic-power reduction from shrinking the process to 65 nm.

formance, lowest power FPGA on the market, with a capacity double that of its 90-nm device.

To address power at the 65-nm node, both companies have attacked the low-power problem on multiple fronts: in circuitry and silicon at the architectural level and in power-savvy design tools to help users manage power in their FPGA designs.

POWER AT 130 NM

Both Xilinx and Altera say that 70 to 90% of the power savings at the 65-nm-process node come from changes to the circuitry and overall FPGA-chip architecture. FPGA vendors started tweaking their circuits and architectures for low power at the 130-nm node—the first node in which leakage became nasty. Derek Curd, senior staff applications engineer at Xilinx, says that starting at the 130-nm node, Xilinx started to become selective about the types of transistors it was using for each area of the device. In the 130-nm Virtex-2 family, the company used one transistor with higher threshold voltage and longer channels for I/O and used a second transistor with a thinner gate oxide for core logic, which operates at high speeds and lower voltages.

Starting with Virtex-4, the company added a third transistor, which had a middle oxide layer that addresses both gate leakage from the gate oxide of a transistor to the substrate and source-to-drain, or subthreshold, leakage (**Figure 1**). "We've traditionally been concerned with subthreshold leakage, but as we go down in process nodes, the gate leakage is becoming a bigger component of the leakage story," says Curd. "At room temperature, it can be two-thirds of the total leakage. You can't control that by making longer channels; you have to do something else. The midoxide gave us a dramatically lower gate-leakage component."

Altera reacted to the need for low power at the 130-nm mode primarily by moving from a traditional, four-input look-up table to adaptive-logic modules, which users can customize to serve their speed-versus-power requirements. Each module contains look-up-table-based resources; two full adders; some carry-chain segments; and two flip-flops, which designers can mix and match to create logic functions with as many as seven inputs in an adaptive-logic module or a mix of two- to five-input logic functions. Altera also uses thicker oxide transistors in I/O, and its foundry, TMSC (www.tmsc.com), moved to a low-k dielectric. Each of these approaches adds another layer of protection against leakage.

Xilinx also saved power on its 90-nm-node devices by placing more standard-cell hard IP (intellectual property) in its FPGA fabric. Xilinx offers three platform FPGAs at the 90-nm node, each containing hard IP for specific applications. It offers the SX ultrahigh-performance, signal-processing platform and the FX embedded-processing and serial-connectivity platforms. Meanwhile, Altera takes a one-size-fits-all approach with the 90-nm-node Stratix II, gaining most of its power savings from its adaptive-logic-module-based architecture. The company last year somewhat followed the Xilinx model by offering the Stratix GX specialized-platform FPGA, which adds high-performance transceiver IP to the

WHAT DRIVES FPGAs' DEMAND FOR LOW POWER?

With power consumption and leakage greater than those of comparably sized ASICs, it is unlikely that FPGAs will soon displace ASICs as the main SOCs (systems on chips) in the next generation of cell phones. According to Tim Saxe, vice president of engineering at QuickLogic, "green" requirements drive much of the demand for low-power FPGAs. "Chances are that you spend more money powering up the clock on your microwave than you do cooking food with it," he says. "When you use it for cooking, it runs at 1000W only for a few minutes, but that little clock is drawing 9 or 10W 24 hours a day. If you can decrease those 9 or 10W to 4 or 5W, you can make a huge difference."

The other factor driving FPGAs to lower power is the fear of overheating. Heat increases leakage, and leakage increases heat. More and more, FPGAs are finding use in applications such as base stations, which can be within units that withstand the elements. This exposure raises ambient temperature. FPGAs may also find use in large, high-speed network equipment. The lack of ventilation, the exposure to sun, or both can increase heat and cause transistors to leak and yield more heat, which leads to thermal runaway and ultimately results in system failure.

Nevertheless, users expect FPGAs to be power hogs in some applications and thus don't lower the power budgets for systems incorporating FPGAs. Vendors such as Altera and Xilinx are stabilizing the power levels of their high-performance FPGAs, doubling capacity, halving die size, and improving performance. All these improvements ultimately allow them to decrease the number of devices in a system.

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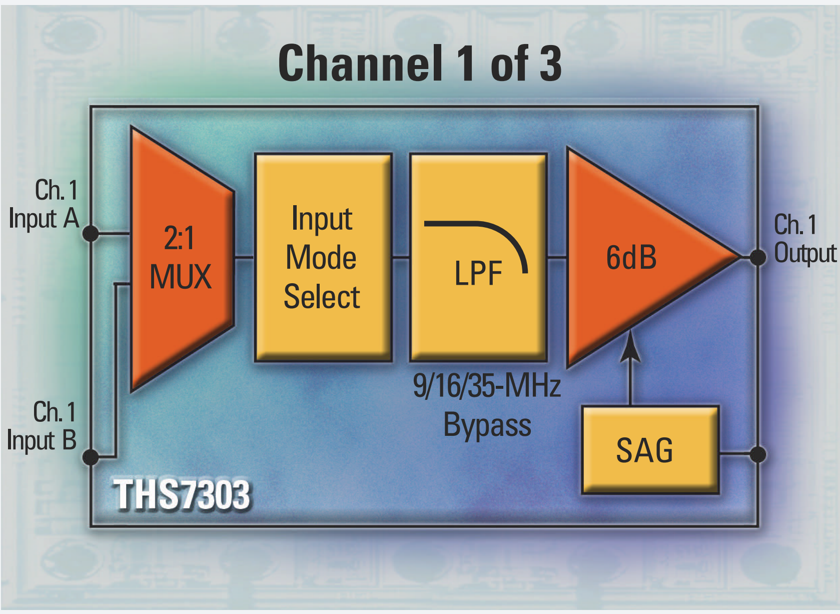

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Stratix II fabric. The company's trump card in low power is HardCopy, which allows customers to mass-produce their devices at lower power in a structured ASIC (**Reference 2**).

To attack power in 65-nm FPGA fabric, both Xilinx and Altera have again significantly changed circuitry and chip architectures. Xilinx has released its V5, and Altera will next year release its 65-nm device.

INNOVATION AT 65 NM

With its 65-nm Virtex-5 FPGA, Xilinx is using a "smarter mix" of its three transistors, but the biggest change is that it steps beyond the traditional four-look-up-table architecture to a new six-look-up-table architecture (**Figure 2**). This approach allows the company to use fewer large transistors because more logic processing occurs inside a look-up table, says Curd. Xilinx has also changed the clustering of these six-input look-up tables. In Virtex-4, each configurable-logic block has four slices, and each slice has two look-up tables and two flip-flops. To reduce power consumption, the V5 has four six-input look-up tables and four flip-flops. The total remains the same at the configurable-logic-block level, allowing the company to employ multiple look-up tables, build larger memories and multiplexers, and build wider functions, according to Anil Telikepalli, senior marketing manager for Virtex products. Xilinx is also adding V5 diagonal routing, similar to Cadence's X-Architecture, as well as traditional, north-to-south, east-to-west routing. "You can now get to the diagonal neighbor directly," says Curd. "One hop gives you lower capacitance than two hops."

The end result is that the V5 has approximately the same leakage as the V4. "If we had done nothing, we would expect a big increase in leakage," says Curd. Xilinx's goal with 65-nm devices is to keep pace with leakage and not follow the predicted upward curve in process and architecture, he says. The V5 has 12 to 40% lower dynamic power than do V4 devices. Most of that dynamic-power savings results from the process reduction, but some of it comes from the architectural changes. Whereas 90-nm devices have 1.2V core power, the 65-nm Xilinx devices have 1V core power. The 65-nm V5 devices also offer about 15% improvement in internal-node capacitance over V4.

"The transistors are getting smaller, so you have fewer parasitics from the transistor itself and shorter distances between logic," Curd says. "Fundamentally, you get a 15% capacitance reduction. When you multiply that figure with the voltage reduction, you get in the neighborhood of a 40% dynamic-power reduction from the process reductions." Curd says that figure can rise to perhaps 50% power reduction if your design maps well into the V5's six-input-look-up-table architecture, which contributes to the dynamic-power savings, too. He says that, if you tune a V5 LX to run at its highest frequency, 550 MHz, it still has 12% less dynamic power than the V4. Part of the device's dynamic- and leakage-power savings results from Xilinx's weaving in hard-IP blocks. Xilinx plans to offer the Virtex-5 LX platform for high-performance logic, the Virtex-5 LXT for high-performance logic with serial connectivity, the Virtex-5 SXT for high-performance digital-signal processing with serial connectivity, and the Virtex-5 FXT for embedded processing with serial connectivity. Xilinx V5 devices require one 1V power supply for core logic, one 1.8 or 2.5V supply for I/O, and a third for auxiliary power.

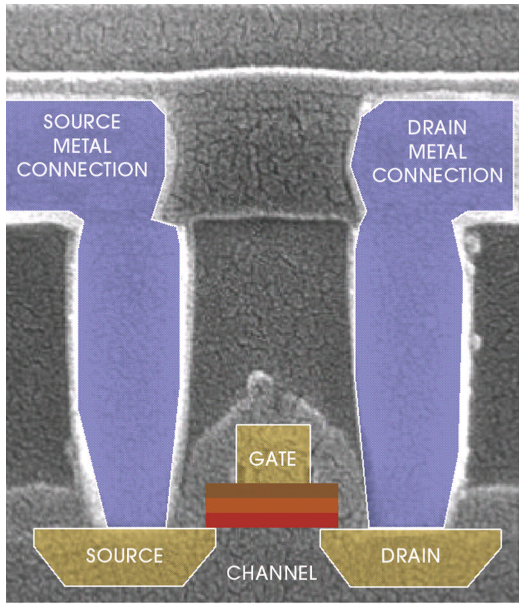

Figure 1 Xilinx's continued use of triple oxide and hard IP helps the Virtex-5 achieve 35% lower dynamic power and maintain the same leakage rate of its 90-nm Virtex-4.

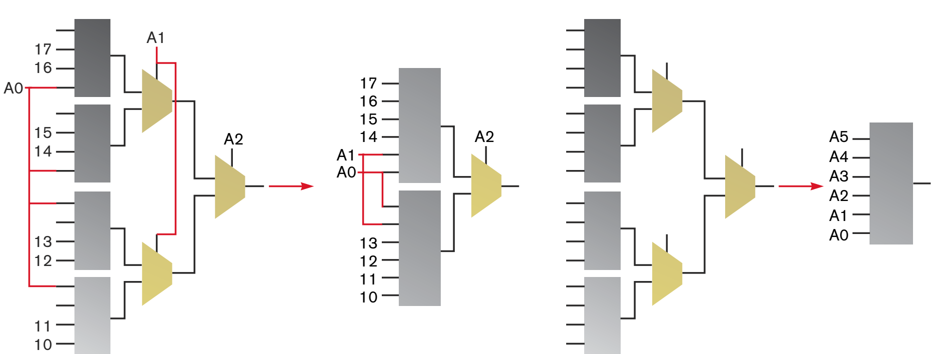

Figure 2 Xilinx's Virtex-5 has a six-look-up-table architecture that reduces the amount of necessary routing and logic levels, which also reduces power.

NOT STANDING STILL

Paul Ekas, senior product-marketing manager for high-end FPGA products at Altera, says that, in creating the architecture for its 90-nm Stratix II FPGAs, the company evenly distributed a mix of power-resistant and thin-oxide transistors throughout the device's fabric. Altera also cranked down the transistors' clocks to save power. Ekas says that, in approaching the 65-nm node, Altera created an architecture that reflects real-world applications that require the

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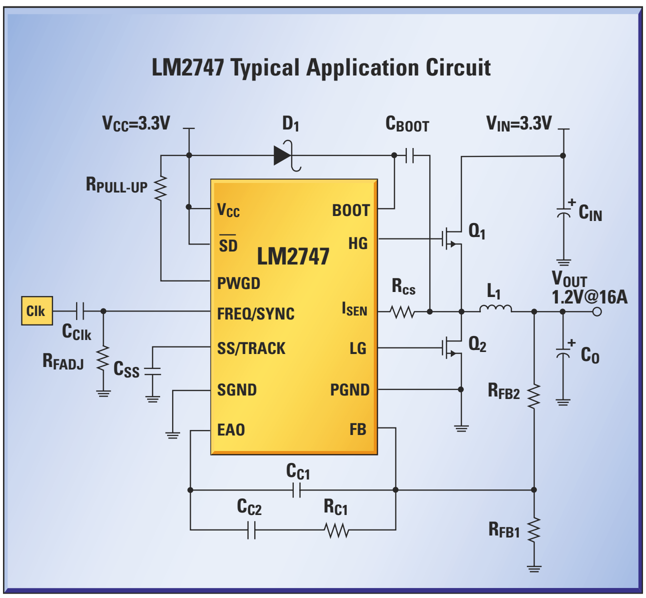

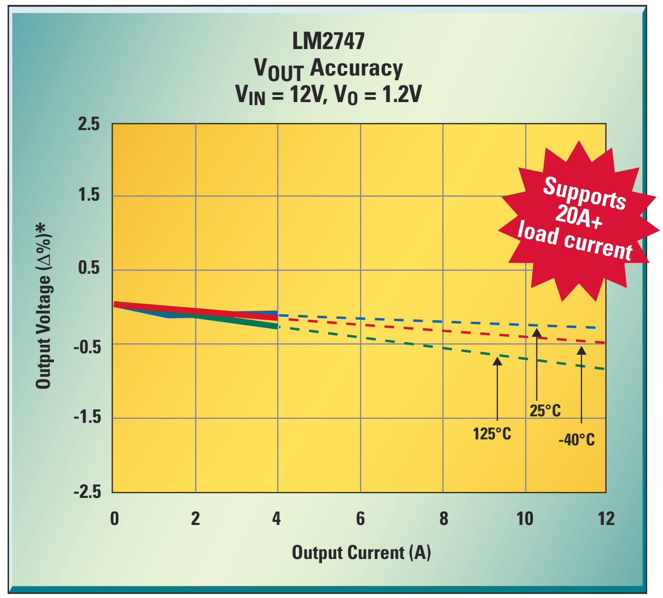

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fastest transistors for the critical path. The rest of the design doesn't require the fastest, most leakage-prone transistors. With Stratix III, Altera complements its high-performance logic elements with new, low-power logic and power-down elements for critical paths (**Figure 3**). "We can change anything that is not the critical path to be low-power logic in the silicon via programming," says Ekas. "During programming, we tell each logic element to be either fast or low-power. For unused logic, you go into power-down mode, making it as little prone to leakage as you can, and you don't route clocks to it, so you isolate it from all signals."

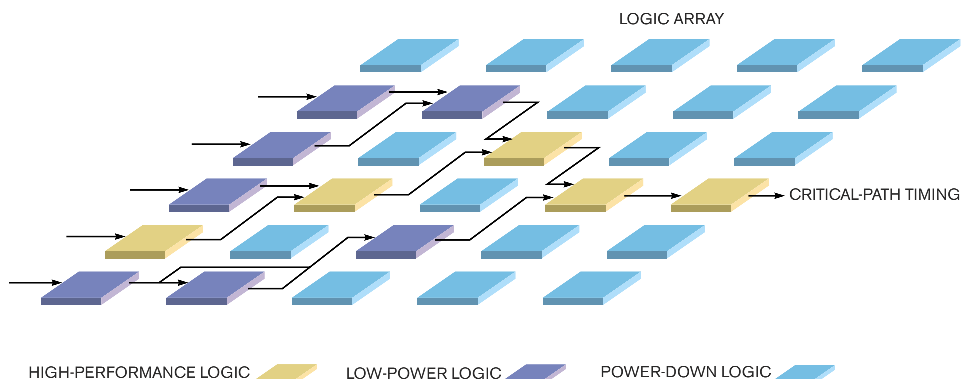

Figure 3 Altera's Stratix III assigns high-performance logic elements to critical paths and low-power logic elements to noncritical paths, and it powers down unused logic elements to reduce leakage.

The Stratix III will have a core voltage of 1.1V and higher standard-I/O voltages, such as 1.8 and 2.5V. "For the baseline 65-nm device, you can use a Stratix II power supply, and, if you add a second power supply, you can add a second core voltage," says Ekas. "If you port a design you implemented in Stratix II to a new Stratix III device, you will see a 50% power reduction. If you raise the clock rate of that design 20%, you see a 30% power reduction, and, if you decrease the clock rate of the design by 30%, you get a 70% power savings."

NEW POWER TOOLS

Both vendors claim that they are adjusting their EDA suites to reduce the number of steps users need to take for managing power. As with their 90-nm offerings, both companies will offer power-estimation, -analysis, and -optimization tools for users concerned about power but whose tool sets automatically manage most of the power. Xilinx's power-optimization tool plugs into the Virtex-5 tool set, and the company is also moving into power-optimized synthesis and physical synthesis. "You get 80 to 90% of the benefit from the architecture itself, but, if you need to scrape off some milliwatts to get into an application, you can use the tool flows," says Curd. Xilinx made its place-and-route algorithms more cognizant of low power. Rather than cluster similar functions in tighter spaces, the router identifies and optimizes those nodes having the highest switching activity to reduce power. "A popular generic approach to saving power is to pack things as tightly as possible to minimize distances and thus minimize capacitance and therefore power," says Curd. "To bring it to the next level, you have to bring in activity rates. What critical nodes have the highest activity rates? Optimizing those will give you the most benefit." The company plans to add more power-enabled tools this summer when it launches the ISE (integrated software environment) Version 8.2 software.

Altera's power-management functions will be automatic, pushbutton features. Altera also offers PowerPlay software in its Quartus II suite for users who need to design for low power. The suite includes a power estimator for use before synthesis and a postroute-power analyzer. A third power tool performs toggle analysis and helps users interconnect and select logic. However, power management isn't the biggest concern for users of Stratix III, says Ekas. "The big challenge for designers is going to be what you can do with another doubling of gates," he says. Doubling the number of gates means that more designers must work on one FPGA project, so Altera is ramping up team-based design software to go with its 65-nm devices.

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Timing closure will also re-emerge as a primary concern for these large devices, so Altera provides the TimeQuest timing analyzer, which features incremental synthesis and a design-space explorer to automatically meet timing constraints. The analyzer runs SDC (Synopsys-design-constraint) format in native mode. Both vendors are also working with commercial EDA vendors to develop power-saving FPGA tools.

TACKLING LOW POWER

Although Xilinx and Altera are taming leakage in their high-end FPGA devices, many vendors offer smaller, slower devices that suit low-power use. Some devices even specialize in low power. For example, Lattice Semiconductor this year introduced its high-performance, high-gate-count, SRAM-based SC (system-chip) family (**Reference 3**). Whereas Xilinx's and Altera's 90-nm parts operate from 1.2V core supplies, designers can tune down the 90-nm Lattice SC family to 1V if customers require power savings. "You get a 50% power reduction if you run it at 1V, and it impacts the performance by only 15%," says Stan Kopec, vice president of corporate marketing at Lattice. "By designing the devices to work over this expanded voltage range, we pro-

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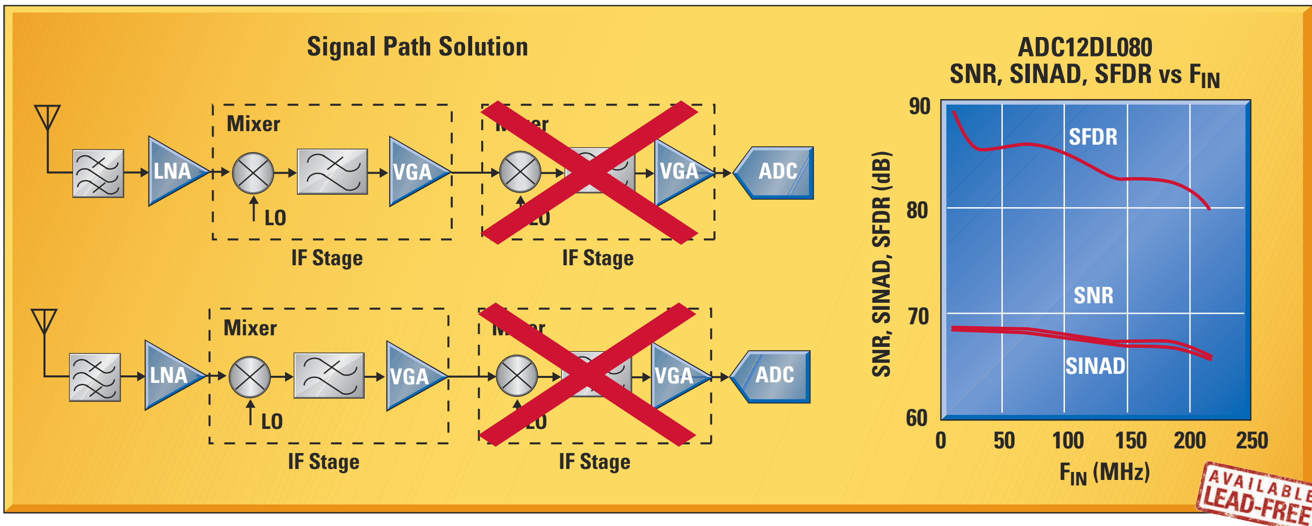

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vide a useful tool to help the system designer dial in performance and power consumption," he says. Both Lattice and Actel also have lineups of nonvolatile FPGAs. The devices have inherently lower power than SRAM-based devices but lack the top performance and capacity of the Virtex and Stratix devices.

Martin Mason, director of silicon-product marketing at Actel, believes that moving to a 65-nm-process node may be a bad move for SRAM vendors. "What are they going to give customers at 65 nm? Is it speed, price, power, or are they going to try to compromise on all three and not do any of them well? Maybe the 65-nm node doesn't bring an awful lot to the party in any of those areas," he says. He asserts that the 65-nm node brings power headaches and that customers, especially those in the "value market," aren't looking for higher performance FPGAs. "From a price perspective, they are pushing the burden onto the board and out of the device," says Mason. He believes that these vendors will increase the total system-cost requirements with additional high-tolerance power supplies, power sequencing, and power management, all of which are driving the analog business to double-digit growth. Actel prefers instead to integrate more of the board and the system by using unique process technology. The company's latest device, Fusion, has a deep-sleep mode, which lets you power it down to 10 μA of standby current (**Reference 4**).

Low power has also become QuickLogic's theme. The company's one-time-programmable, antifuse PolarPro and Eclipse II devices require little current and act as gatekeepers to power down power-hungry devices when not in use (**Reference 5**).EDN

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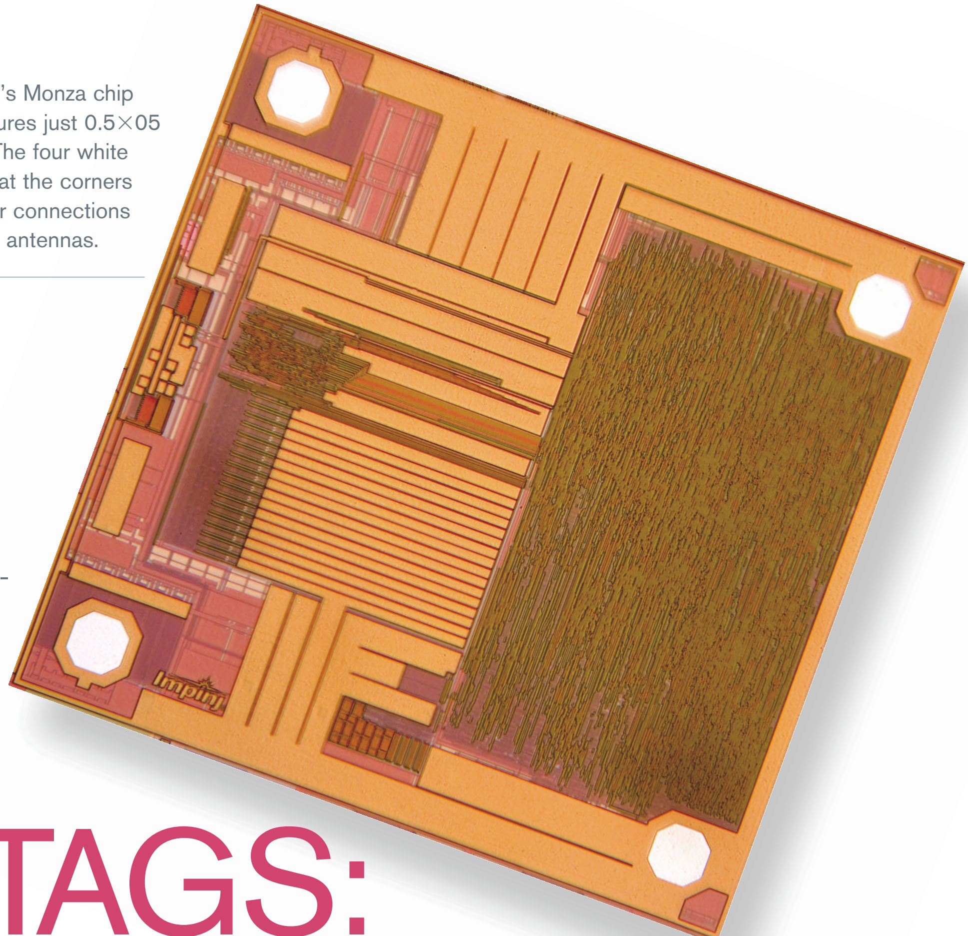
Impinj's Monza chip measures just 0.5×05 mm. The four white pads at the corners are for connections to the antennas.



RFID-TAG PRICES HAVEN'T YET REACHED THE MAGICAL 5-CENT MARK, BUT AGGRESSIVE CHANGES IN TECHNOLOGY ARE PUSHING DOWN THEIR COST AND IMPROVING PERFORMANCE.

RFID TAGS: DRIVING TOWARD 5 CENTS

BY CHARLES J MURRAY • TECHNICAL EDITOR, *DESIGN NEWS*

Makers of RFID chips and so-called inlays, which include the chip, antenna, and substrate, have been trying for years to reduce prices for RFID tags to 5 cents. However, these manufacturers hesitate to do so because those less expensive tags may lack the capabilities of their more expensive counterparts. "We've been talking about the mythical 5-cent price point for years," notes Mike Liard, RFID-practice director for Venture Development Corp. "Is it possible? Yes. But it may not necessarily be the type of tag you're looking for." As a result, most manufacturers haven't rushed to put 5-cent tags on the market. Instead, they've been content to cut prices at a steady rate of about 5 to 10% per year since 2000 while improving the technology. As a result, users of the tags are employing them in applications no one dreamed of a decade ago, despite their inability to reach the elusive nickel price.

At McCarran International Airport in Las Vegas, for example, operators attach "bag tags" with dual dipole antennas to luggage to ensure that RFID readers in the handling system can communicate with all bags, no matter their orientation on conveyor belts. The technology, which Symbol Technologies developed, integrates two antennas 90° from one another; thus, the RFID tags can communicate with the airport's RFID readers, no matter how baggage handlers toss the luggage onto conveyor belts. "If you wanted to have a lower cost solution in which one antenna would work, the bags would have to be oriented in a certain way, and they'd have to pass the reader in a certain way," says Alan McNabb, senior director of product management for Symbol's RFID tags. "But with our tag, the orien-

AT A GLANCE

- Adoption of RFID lags behind forecasts, partially because potential users don't understand the benefits of RFID.
- Currently, 5-cent RFID tags lack the capabilities of their more expensive counterparts.
- Process changes take time, especially when they involve retraining people and reprogramming machines.
- Developing the infrastructure for RFID calls for major capital investment.

tation of the bag doesn't matter."

Such dual-antenna tags haven't reached rock-bottom prices, but at roughly 20 cents each, they offer capabilities nickel tags can't match. Similarly, retailers have begun using tags with specialized antennas to enable garments buried in stacks to successfully "talk" to RFID readers. Again, cheaper tags are unlikely to achieve such feats.

The bottom line is that while RFID vendors have been lowering their prices and improving their technology, they've been carving out new niches for themselves. Increasingly, RFID tags are finding use on pallets, cartons, garments, luggage, DVD cases, pill bottles, and library books. And experts foresee their future use in low-cost, everyday items—from lipstick cases to cereal boxes. Although they won't soon replace bar codes, they nevertheless offer non-line-of-sight capability, which means that they can gather information on their whereabouts without the need for individual handling. As a result, they can deter theft and counterfeiting.

"RFID is not labor-intensive," notes Sanjay Sarma, associate professor of mechanical engineering at the Massachusetts Institute of Technology and research director for MIT's Auto-ID Center. "It gives you information you can't get with a bar code, unless you have an army of people scanning every product."

COST STILL KEY

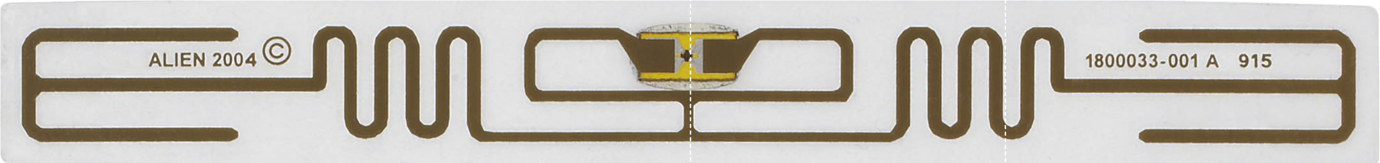
At costs of 10 to 20 cents apiece, however, RFID tags are still far more expensive than bar codes, which is why the drive to 5-cent tags continues. "The state of momentum within the industry toward the 5-cent mark is healthy," Sarma says. "The good news is that it has gone beyond research. It's moved into development, and a lot of companies are looking to go to 5 cents."

Whether 5 cents is their ultimate goal, makers of chips and inlays alike have targeted lower cost. Chip designer Impinj Inc, for example, is cutting costs through a novel semiconductor approach that enables the company to apply low-cost CMOS techniques to RFID devices. Unlike conventional RFID-chip makers, which typically use extra photo masks and process steps to create onboard, nonvolatile EEPROM or flash memory on RFID chips, Impinj engineers use "self-adaptive silicon." Using the technique, they create special transistors containing gates that store bits of memory. By fabricating such transistors, they can make nonvolatile memories without resorting to the extra photo masks and steps that EEPROMs and flash memory require. "Self-adaptive silicon enables us to make nonvolatile memory with the simplest of CMOS processes," says Dimitri Desmons, vice president of marketing for Impinj.

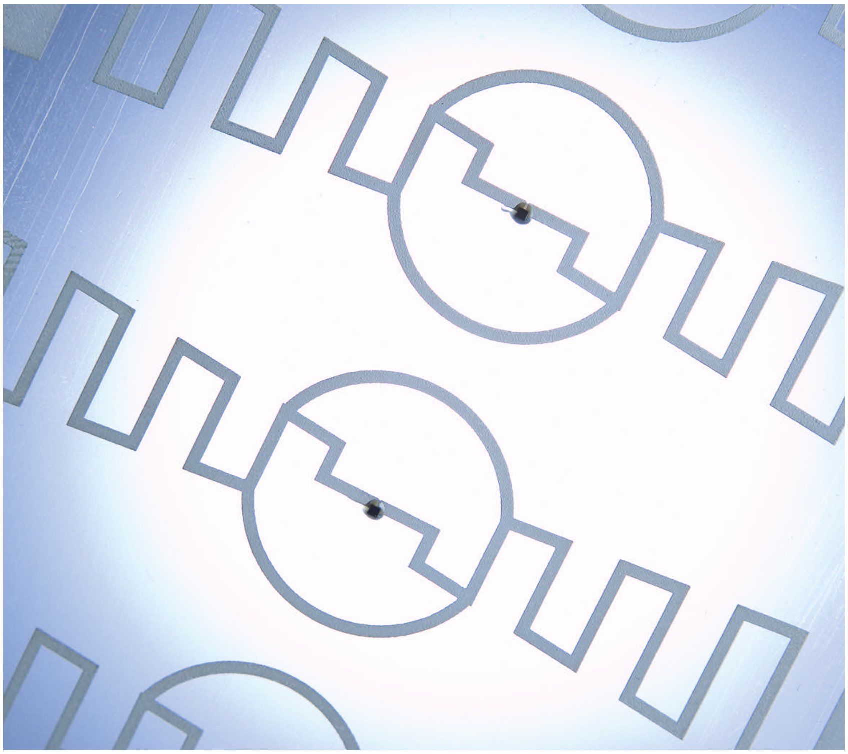
Impinj engineers say that self-adaptive technology can potentially cut pennies from chip costs. Moreover, such technologies even further reduce costs when manufacturers combine them with high-volume-assembly methodologies, such as those that Alien Technology developed. Alien, which employs FSA (fluidic self-assembly), recently cut inlay costs to 12.9 cents each. A company founder developed the technique, which he thought of while playing a child's game that required him to maneuver steel balls into tiny slots. The technique allows the company to package as many as 2 million chips per hour into RFID tags, compared with 10,000 per hour using conventional methods. The trick, the company says, is to suspend the tiny semiconductor devices in a liquid and then "flow" them across the holes; the devices then drop into these holes and self-align. The self-assembly technology combines with growing production volume to enable Alien to cut its tag costs by nearly 50%, down from 23 cents each.

Other vendors have attacked the cost issue from a different perspective. Symbol Technologies, for example, has cut the

Tracking of pallets, a traditional staple of the RFID market, could benefit from price reduction targeting consumer RFID.



Alien Technology's low-cost Squiggle tag uses fluidic self-assembly to package as many as 2 million chips per hour.



Impinj's "propeller" inlay targets UHF frequencies in different countries without charging the chip or the antenna.

cost of its tags through multiple efforts, not the least of which is its move from silver to aluminum antennas. The company, which makes high-performance RFID systems, moved from the higher conductivity of silver to the lower conductivity of aluminum by developing an on-chip "charge pump" that helps boost the continuity and strength of RF signals coming to the antenna.

AN INTERNET OF THINGS

Such technologies are making inroads for RFID. Symbol, for example, has placed similar technologies on pill bottles for the counterfeit-wary pharmaceutical industry. "The pharmaceutical industry has a huge issue with counterfeit products coming through the market," says Dirk Morgenroth, marketing manager for RFID at Philips Semiconductors. "They've been very vocal about using RFID."

Manufacturers, including Philips, Texas Instruments, Impinj, and Alien, have also placed their RFID products on shirts, pants, and sweaters in the fashion industry, as well as in library books and on DVD and CD cases. The industry's biggest score to date, however, could be in the works in Europe, where rumor has it that the European Central Bank (www.ecb.int) is working with vendors on weaving RFID into the fabric of its bank notes. The technology, most probably for incorporation into larger bills, would enable money to carry its own history. Hence, it would become more difficult for kidnapers to ask for unmarked bills. It would also enable law-enforcement agencies to "follow the money" in illegal transactions.

The project, which *Wired* and *EE Times* originally reported, was supposed to take effect in Europe's 2005 currency. Hitachi Ltd, which announced in February that it has developed the world's smallest RFID chip, measuring just 0.4×0.4 mm×7.5 microns, has frequent links with the European reports. Hitachi, however, denies it has worked on such a project. A European Central Bank spokesman says, "We cannot say anything about this, and we've requested that our providers sign a mutual agreement not to talk about it."

Even if such projects never reach fruition, however, experts are confident that RFID will eventually be the backbone of a plan that researchers call an Internet of things. In this scenario, almost everything, large and small, connects through the Web. The plan, which hardware and software protocols describe, calls for all information on a product to be written in a code based on XML (Extensible Markup Language). The code, which forms a Web page for each item, would connect through RFID tags to Internet servers. Thus, anyone in any location could instantly identify all products. A broad coalition of corporate giants, including Coca-Cola (www.cocacola.com), International Paper (www.internationalpaper.com), Johnson & Johnson (www.jnj.com), Kimberly-Clark (www.kimberly-clark.com), Pepsi (www.

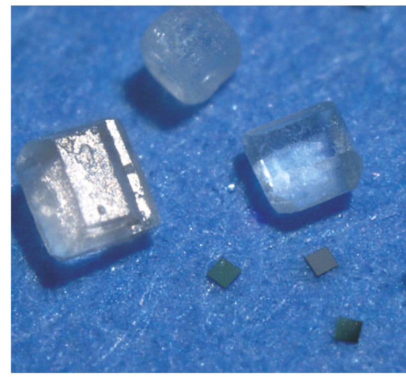
Symbol Technologies' "bag tags" use dual dipole antennas to ensure that scanners can read each bag as it moves along airport conveyor belts.

"THESE RFID TECHNOLOGIES WILL COEXIST WITH THE BAR CODE FOR A LONG TIME INTO THE FUTURE, BUT THEY WILL PROVIDE INFORMATION THAT A BAR CODE CAN'T: 'DID THE ITEM GO TO THE SALES FLOOR?' YOU CAN'T KNOW THAT WITH A BAR CODE."

pepsi.com), Procter & Gamble (www.pg.com), and others, have supported such efforts through MIT's Auto-ID Center.

Low cost is key to such plans, but researchers have worked that out, too. Ultimately, they say, everyday items will incorporate RFID, not on sticky tags, but through integration into the corrugate of cardboard boxes. Ongoing effort in this area will be one of the keys to lowering RFID cost, researchers say, because the technology eliminates the need for certain parts of the tag. Manufacturers would integrate such technologies during the cardboard-manufacturing process, thus enabling cost reduction.

"These RFID technologies will coexist with the bar code for a long time into the future," says Sarma of MIT. "But they will provide information that a bar code can't: 'Did the item go to the sales floor? Did the meat sit in the fridge long enough?' You can't know that with a bar code." Sarma says such technologies will become widespread when production volume reaches a tipping point. When that scenario happens, it will drive costs down to a level low enough to motivate use of RFID on everyday items. And with retailers—particularly Wal-Mart (www.walmart.com)—pushing for RFID, the concept is realistic, experts say. "The question now is the tipping point," Sarma says. "When do you get to the percentage that causes you to say, 'I'm going to put the tag inside the corrugate?' In the next year, we could see it happen."EDN



Grains of salt dwarf Hitachi's µ-Chip, which measures just 7.5 microns thick.

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36V Input DC/DC Converters

High Performance Analog Solutions from Linear Technology

Automotive batteries, industrial power supplies, distributed supplies and wall transformers are all sources of wide-ranging high voltage inputs. The simplest method to step-down these varying sources is to use a monolithic step-down regulator that can directly accept a wide input range and deliver a well-regulated output. A group of Linear Technology's growing family of high voltage DC/DC converters accept inputs from 3.6V to 36V (or higher) and provide excellent line and load regulation and dynamic response. Nevertheless, these mid-range converters are acceptable for a wide range of applications; however, we also offer higher voltage products with inputs up to 80V. In many automotive applications, these parts are required to meet a minimum input voltage scenario, known as cold crank, where the cars battery voltage can drop to 4V, yet a regulated 3.3V is required on the output. Similarly, during a load dump scenario, transients of 36V and higher can be found at the input of the DC/DC converter which is required to regulate at a constant voltage. All of the devices offer a high efficiency solution over a wide load range with a well regulated output. The LT®3481 can deliver up to 2A of output current and offers Burst Mode® operation with quiescent current of only 50µA while the LT3493 and LT3505 can deliver up to 1.2A from a very tiny solution footprints which utilize minimal external components. See Figure 8 for a profile of our high voltage monolithic buck.

36V, 2A Step-Down Requires only 50µA Quiescent Current

The LT3481 is available in a 10-lead 3mm x 3mm DFN (or MSOP) package with an integrated 3.8A power switch and external compensation for design flexibility. The switching frequency is user programmable from 300kHz to 2.8MHz. Figure 1 shows a schematic of the LT3481 capable of producing 3.3V at 2A from an input of 4.5V to

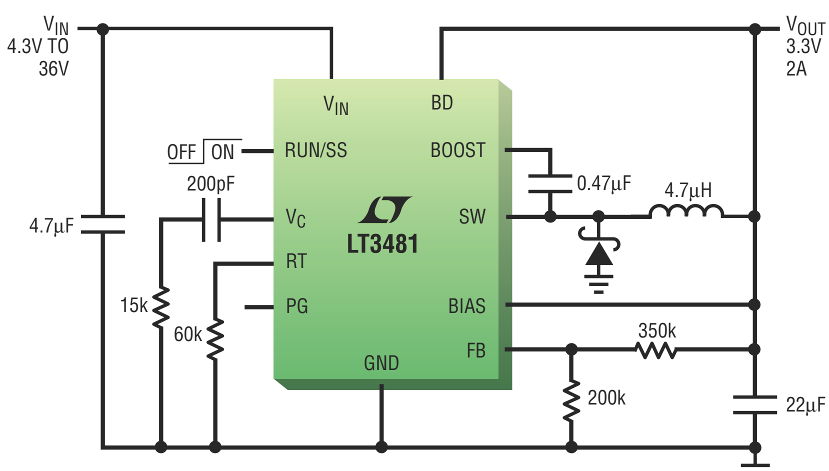


Figure 1. The LT3481 800kHz, DC/DC Converter Delivers 2A at 3.3V Output

36V Input DC/DC Converters

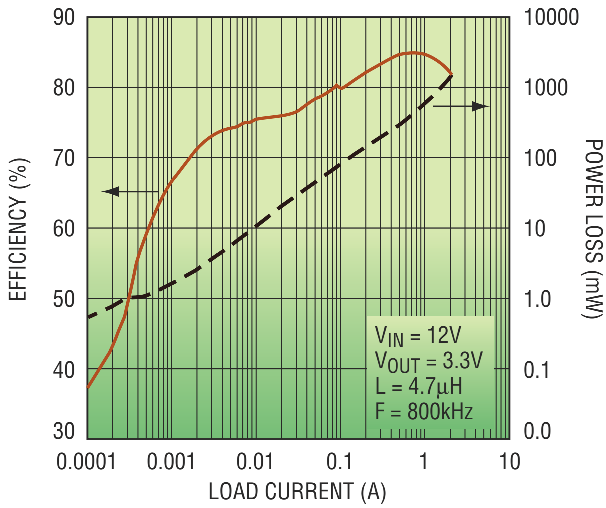


Figure 2. Efficiency vs Load Current for Figure 1 Circuit

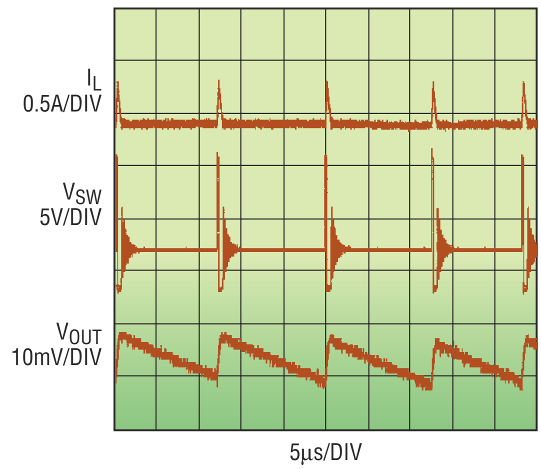


Figure 3. LT3481 Burst Mode Operation at 10mA Load Current With V_{IN}=12V For Figure 1 Circuit

36V while Figure 2 shows resultant efficiency of the circuit (with V_{IN}=12V nominal).

The LT3481 utilizes a unique low ripple Burst Mode operation which maintains high efficiency at light loads while keeping the output voltage ripple below $15mV_{PK-PK}$ (Figure 3). Low noise operation can be critical if there are any noise-sensitive circuits such as wireless transceivers close by. During Burst Mode operation, the LT3481 delivers single cycle bursts of current to the output capacitor followed by sleep periods when the output power is delivered to the load by the output capacitor. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 50µA. Figure 3 shows the inductor current and output voltage ripple under single pulse Burst Mode operation from 12V input to 3.3V output. As the load current decreases to a no load condition, the percentage of time that the LT3481 operates in sleep mode increases and the average input current is greatly reduced resulting in high efficiency. The LT3481 also has a very low shutdown current (less than 1µA) that significantly extends battery life in applications that spend long periods of time in sleep or shutdown mode.

Additionally, the LT3481's high side bootstrapping boost diode is integrated into the IC to minimize solution size and cost. When the output voltage is at least 2.8V, the anode of the boost diode can be connected to output. For output voltages lower than 2.5V, the boost diode can be tied to the input. For systems that rely on a well-regulated power source, the LT3481 provides a power good flag that signals when V_{OUT} reaches 90% of the programmed output voltage. Finally, a resistor and capacitor on the RUN/SS pin programs the LT3481's soft-start, reducing maximum inrush current during start-up.

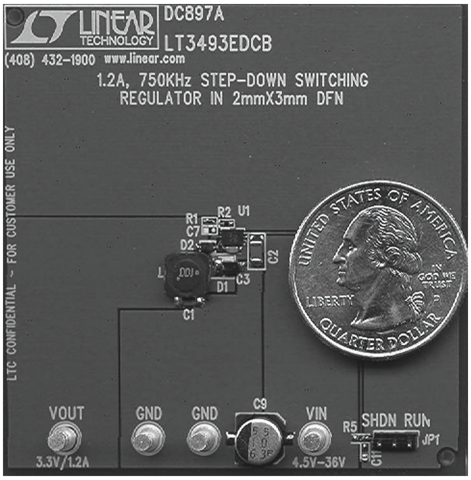


Figure 4. LT3493 Demo Board Showing <50mm² footprint

36V Step-Down DC/DC Converters Deliver 1.2A from 50mm²

Both the LT3493 and the LT3505 include an internal 1.75A, 36V power switches which are capable of withstanding 40V transients. Both parts deliver efficiencies as high as 85% from 12V inputs. Their 0.78V reference voltage enables them to operate with output voltages as low as 0.8V. Both parts offer cycle-by-cycle current limit, providing protection against shorted outputs and soft-start eliminates input current surge during start-up. The low current (<2µA) shutdown mode

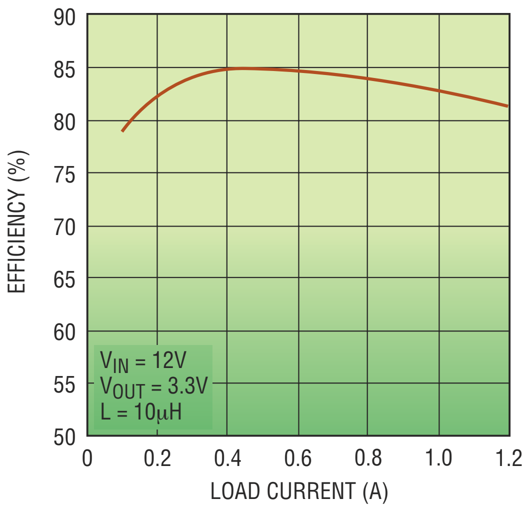


Figure 5. LT3493 Efficiency vs Output Current Curve

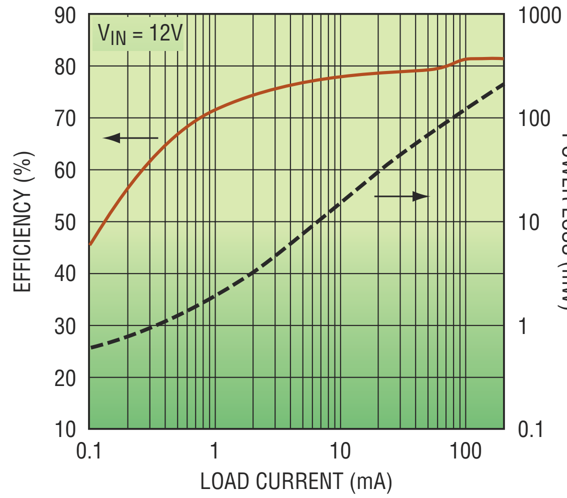


Figure 6. LT3470 Efficiency and Power Loss vs Load Current

provides output disconnect, enabling easy power management in battery-powered systems.

The LT3493 operates with a switching frequency of 750kHz in a 6-pin DFN package (2mm x 3mm). Its internal loop compensation eliminates the need for external compensation components, reducing the PC board space to less than 50mm^2. Figure 4 shows the actual size of the LT3493's solution footprint. This particular circuit generates 3.3V from a 12V input and delivers up 1.2A of output current.

The LT3505 operates with a switching frequency that is user-programmable from 250kHz to 3MHz. This enables designers to keep switching noise out of critical noise sensitive circuits while using the smallest external components possible. It is packaged in a 3mm x 3mm DFN-8 offering a very compact 36V input capable solution.

40V Step-Down Converter Deliver up to 200mA from a ThinSOT

The LT®3470 is a 40V step-down converter with the power switch, catch diode and boost diode integrated in a tiny ThinSOT™ package or 2mm x 3mm DFN. The boosted NPN power stage provides high voltage capability, high power density and high switching speed without the cost and space of external diodes.

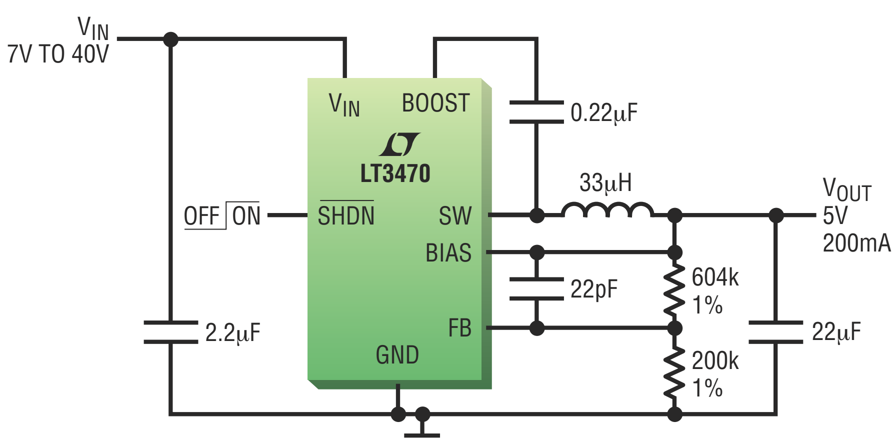


Figure 7. LT3470 Circuit for 40V Input to 5V at 200mA

36V Input DC/DC Converters

The LT3470 accepts an input voltage from 4V to 40V and delivers up to 200mA to load (Figure 7). Micropower bias current and Burst Mode operation enable it to consume merely 26µA with no load and a 12V input. Hysteretic current mode control and single-cycle bursts result in very low output ripple and stable operation with small ceramic capacitors. The combination of small circuit size, low quiescent current and 40V input makes the LT3470 ideal for automotive and industrial applications.

The LT3470 uses a hysteretic current control scheme in conjunction with Burst Mode operation to provide low output ripple and low quiescent current while using a tiny inductor and ceramic capacitors. The switch turns on until the current ramps up to the level of the top current comparator, then turns off and the inductor current ramps down through the catch diode until the bottom current comparator trips and the minimum off-time has been met. In continuous mode, the difference between the top and bottom current comparator levels is about 150mA. Since the switch only turns on when the catch diode current falls below threshold, switching frequency decreases, keeping switch current under control during start-up or short circuit conditions. If the load is light, the IC alternates between micropower and switching states to keep the output in regulation. Hysteretic mode allows the IC to provide single switch-cycle bursts for the lowest possible light load output voltage ripple (<20mV$_{PK-PK}$) from 12V to 3.3V at zero load.) During continuous switching mode at higher current levels, the output voltage ripple is even smaller (<10mV$_{PK-PK}$).

The LT3470's high level of integration, wide input voltage range and very compact solution footprint make it ideal for step down applications which require up to 40V inputs and less than 200mA of load current.

Figure 8. High Voltage Monolithic Buck Family Showing Input Voltage vs Output Current

BY MARK GERBER, TEXAS INSTRUMENTS • MOODY DREIZA, AMKOR TECHNOLOGY

Stacked-chip-scale-package-design guidelines

DESIGN OPTIMIZATION HELPS TO AVOID MANUFACTURING PROBLEMS, TO MAXIMIZE PRODUCT PERFORMANCE, AND TO ACHIEVE LOWEST PACKAGING COST.

You can configure the die stack for S-CSPs (stacked-die chip-scale packages) in multiple ways. However, using design guidelines can help you use die stacking for laminate-based and wire-bonded S-CSPs with more than 200 I/O pins. These packages typically find use in handheld products. When stacking mixed-technology dice, such as ASICs and memory, the challenge is often how to deal with wire-bond density. Wire-bond design must maximize the space between adjacent wires and minimize wire sweep—that is, wire misalignment in the horizontal plane. Wire sweep is undesirable because it can affect the inductance of adjacent wires, create noise, or cause a short when wires touch. Wire-sweep problems can occur at various stages during the wire-bonding process.

The two most common wire-bonding- and wire-loop-control methods in S-CSP assembly are conventional ball bonding and "reverse" SSB (standoff-stitch bonding). In conventional ball bonding, the first bond is to the die pad, and the second is to the substrate finger. In SSB, the first bond is to the substrate finger, and the second is to a stud on the die pad. SSB addresses die-to-die bonding and provides higher wire loops. However, SSB is by nature more prone to wire-sweep problems occurring at heat-sensitive zones, raising the risk of wire breakage. Also, the longer SSB wires are more prone to stitch misplacement and wire sagging.

In general, longer wires increase the risk of wire sweep. For a given distance between a die pad and a substrate finger, SSB results in a longer wire than that for conventional ball bonding. You should avoid SSB in S-CSP design, instead using conventional wire bonding whenever possible. Conventional wire bonding is also advantageous because it has a throughput approximately 1.5 times higher than SSB, helping to lower manufacturing cost. Overall, S-CSP design should minimize wire length by optimizing the substrate's bonding-finger location to minimize pad-to-finger distances.

With S-CSP, wire crossing can create the risk of yield loss from wire shorts, and you must take care to minimize wire crossing through the die and the substrate. Proper management of wire crossing at package design means that you will avoid wire crossing. However, when you cannot avoid wire crossing, place crossing wires within a design-safety zone. In a design-safety zone, you can, for example, maximize the spacing between crossing wires and maintain reasonably high wire loops. You can achieve these design goals by proper bond-finger placement.

In **Figure 1**, some of the lower (green) wires cross under the upper (purple) wires at points close to second-bond termination, at which the upper wires bond to the die pads. This situation creates a risk of wire shorts from wire sweep. To optimize this design, designers relocated the bonding fingers for the lower wires closer to the die edge. Although wire crossing still exists, the modified design puts the crossing points close to the middle span of the upper wire tier, thus increasing wire spacing where the wires cross.

In many cases, staggered rows of bond fingers, rather than one row, help reduce wire crossing: Bond fingers on the substrate for the lower die reside on the inner row, and bond fingers for the upper die reside on the outer row. The loop height of both wire tiers must then achieve sufficient spacing between both tier wires.

DIE LOCATION AND STACKUP

The location of one die with respect to the other is critical in many respects. For example, a designer may be able to significantly shorten bond wires just by shifting die location or achieve more die-to-die bonding by moving one die respective

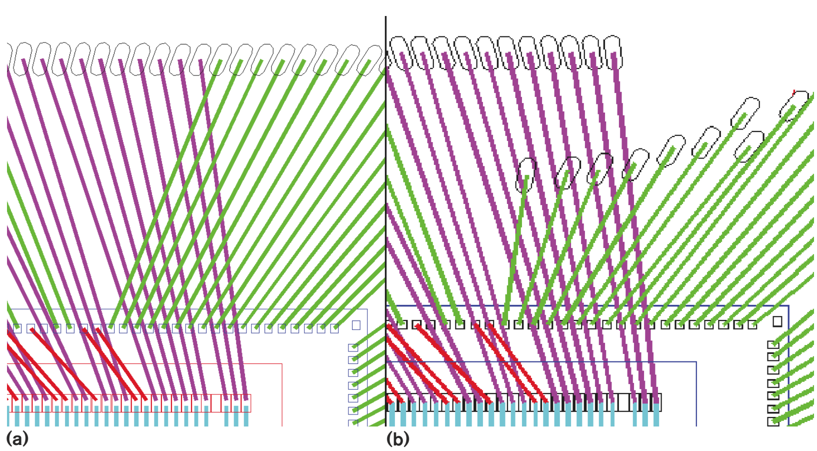
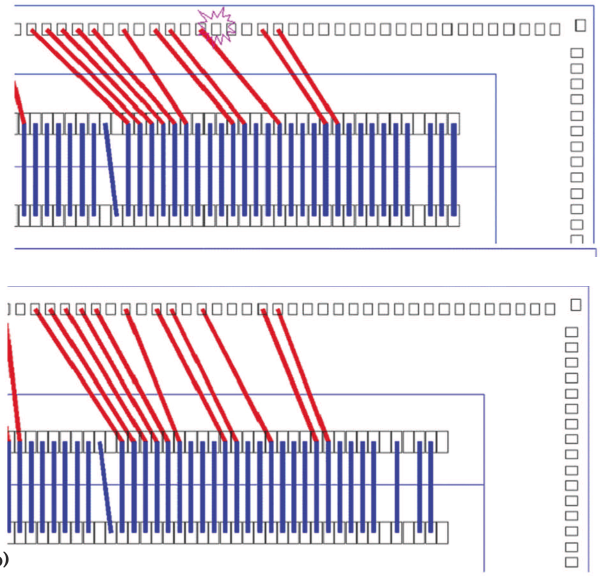


Figure 1 A substrate-design change minimizes wire crossing by placing touch-prone wire crossings close to the second bond termination (a) and moving them to the midspan of the upper wire (b).



(b)

Figure 2 You can avoid a shorted wire (a) by shifting relative die location (b).

to another (**Figure 2**). During the bonding operation, the trajectory of the wire-bond capillary often swings backward—that is, opposite from the direction of the second bond—to create the desired loop in the wire. With S-CSP, die-to-die bonds often exist, as does a risk that capillary movement might interfere with previously bonded wires. You can avoid such interference through wire-loop and wire-bonding-sequence design.

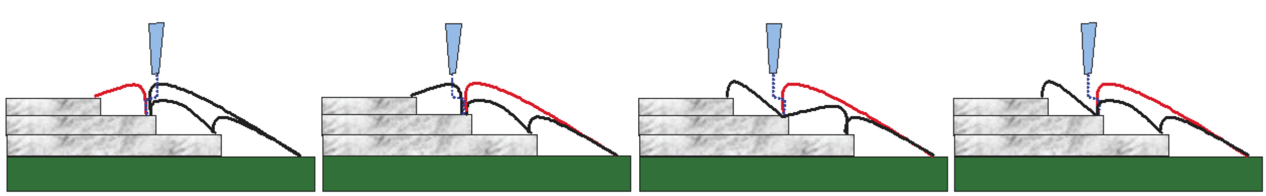
Several three-die stack-wiring options exist. The options in **Figure 3a** and **b** result in capillary interference. You can avoid this interference with the wire loops and bonding sequences (**Figure 3c** and **d**). In addition, wire-loop and -bonding sequence influences die-pad size, so you must consider these factors early in the die-design stage of IC development. Wireless-system applications typically dictate aggressive low-profile S-CSP specifications. It is critical to perform a die-stackup analysis during package design to understand wire-bonding requirements. Low-loop wires ensure a sufficient wire-to-mold-top surface and good mold flow. Sufficient mold-compound thickness above the die avoids yield loss from incomplete fill, mold void, and excessive wire sweep during molding.

The effect of wire length on electrical performance is critical. Resistance increases from wire length are dramatically higher than increases in substrate-trace lengths. In addition, using smaller diameter wire results in higher resistance. Stacked-die packages, especially those with pyramid die stacks—that is, smaller die on larger die—have longer wire runs that you must carefully consider. By optimizing bond-finger placement and adopting chamfered corners on bond fingers, you can reduce wire resistance by reducing wire length. In addition, die-to-package orientation may help to alleviate wire-length issues, but you must carefully consider this orientation to avoid creating other problems. Designing for high performance requires consideration of critical nets as constraints; you should optimize the pinout, finger placement, and routing of the critical nets before those for noncritical nets. A co-design effort is critical for optimized package electrical performance.

STACKING SEQUENCE

Design issues to consider for die stacking include trade-offs between pyramid stacking and same-size-die stacking—that is, stacking equal-sized or larger die on another die when an inter-die spacer enables access to pads on the lower die. When a small ASIC die has strict performance requirements, you should locate it at the bottom of the stack, so that it can use shorter wires (**Figure 4**). A fundamental goal of stacked-die packaging is to lower cost to the end user by reducing board space and component count. For the end customer, the objective is to create more integrated packaging using methods, such as stacked-die packaging, that translate into lower cost and a smaller form factor for the product. However, stacked-die packaging is not inherently less costly. Advanced package suppliers face a number of issues surrounding die stacking, including die and assembly yields, additional assembly costs, increased logistical costs, and increased material costs. You must carefully manage these items so that the end products both work correctly and provide adequate profit margins.

Die and assembly yields are the most critical factors when estimating the cost feasibility of multidie packaging. However, other factors also can have a significant impact on the total-cost model. These factors, which tie closely to the concept of design for manufacturability, center on the substrate: the main component of the package. Rigid CSP substrates commonly find use in wireless- and handheld-system applications because of their versatility in routing and density capabilities. Over the last several years, significant improvements have emerged in laminate-substrate technologies to adapt to the developing needs of handheld systems. Single-die laminates have focused on improving bond-finger pitch, and the silicon designers have targeted improving the bond-pad pitch. With greater I/O counts and



(a) (b) (c) (d)

Figure 3 In a three-die stack, wire-loop-sequence options include those with capillary movement (a and b) and those without capillary interference (c and d).

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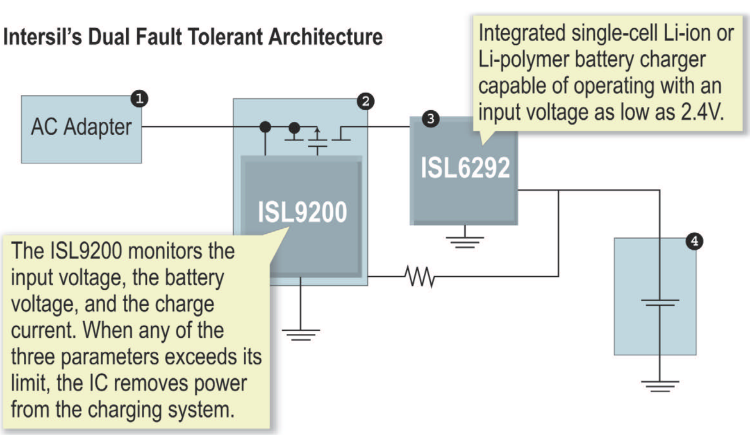

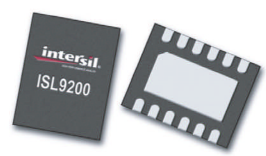

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POTENTIAL FAILURES				Consequence of Dual Failure
❶	❷	❸	❹	
●	●			❸ will fail but the protection module in the battery pack will protect the battery cell.
●		●		Both ❷ and ❹ will protect the battery cell.
●			●	❸ will limit the battery voltage. ❷ has an additional level of protection.
	●	●		The protection module in the battery pack protects the cell.
	●		●	❸ will limit the battery voltage to 4.2V, within 1% error.
		●	●	❷ will sense an over voltage case and remove the power from the system.

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smaller package-substrate areas, all the main-substrate technological parameters have improved. These parameters include metal lines and spacing, via diameter and capture-pad sizes, substrate-core thicknesses, multilayer advancements, metal-plating improvements, and solder-mask enhancements.

When using rigid laminate substrates for die stacking, several factors drive the need for and use of advanced technology rules that can ultimately drive up final substrate cost. With a good understanding of these design considerations and cost trade-offs, you can ultimately minimize the total package cost and bring it close to that of a single-die approach. Stacked-die-substrate designs

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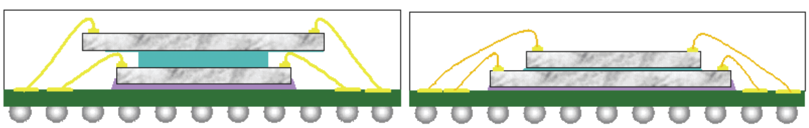
with unique individual dice generally require increased routing density on the top metal layer of the substrate. You can control this increased trace density through a carefully managed co-design effort for each die in a stack. For example, with co-design, you might use the signal layout on one of the two dice as a foundation for die layout. In the best-case scenario, you can die-to-die wire-bond all of the same signals between dice, thus



(a) (b)

Figure 4 When the performance of the smaller die is important, the same-size stacking option (a) gives better performance than the pyramid-stacking option (b).

eliminating the need to use the substrate to interconnect the two dice. Ultimately, this approach enables the lowest cost substrate design and simplifies manufacturability when other key design factors are in place.

As it becomes more difficult to directly bond stacked-die signals to each other, you may need additional bond fingers to relay a signal from one die to the other. Increased bond-finger density often implies increased substrate cost. In addition, you may be able to use a smaller diameter wire. This approach will increase resistance per millimeter run of wire and tighten overall wire-length constraints. For designs in which having multiple rows of bond fingers is not feasible, designers must consider the effects of narrower finger pitch on substrate cost, wire size, wire length, and wire electrical effects.

DIE-STACKING SEQUENCE

When stacking two die of approximately the same size, you might use a spacer to avoid interference between the top die and wires on the bottom die. However, the die-stacking sequence in-

volves trade-offs. First, when you place the die with significantly more wires on the bottom of the stack and place its associated bonding fingers in the inner row, you can expect small bonding-finger pitch. On the other hand, when you place the die with significantly fewer wires on the bottom, you can expect greater bonding-finger pitch because the bond fingers for the die with denser wires are in the outer row, which allows placing bond fingers at a more desirable larger pitch (**Figure 5**).

Overall, S-CSP-design approaches maximize yield, performance, and reliability and minimize cost. These approaches include choosing conventional wire bonding over SSB, optimizing substrate-bond-finger placement to minimize wire length and reduce the risk of wire sweep, and reducing the risk of wire shorts by moving wire-crossing points to the midspan of upper tier wires. These approaches also include optimizing critical nets before routing other nets, avoiding capillary interferences with adjacent wires, placing higher performance die at the bottom of a stack, and placing die with fewer wires at the bottom to allow greater bond-finger pitch and lower substrate costs. EDN

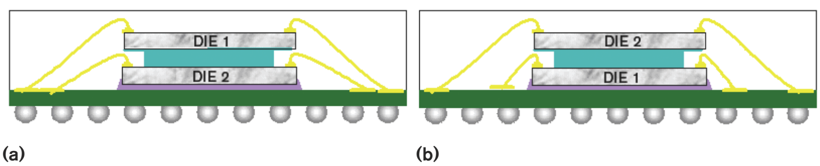


Figure 5 Die 1 requires significantly fewer wires than Die 2. Placing Die 2 on the bottom (a) results in smaller bond-finger pitch, but placing Die 1 on the bottom results in a larger bond-finger pitch (b).

AUTHORS' BIOGRAPHIES

Mark Gerber is an advanced-package-productization manager at Texas Instruments (Dallas). His responsibilities include design, development, and release of product introductions for advanced package designs that support strategic business-unit entities, such as wireless, high-performance analog, ASIC, and broadband. He has a bachelor's degree in mechanical engineering from Texas A&M University (College Station, TX) and is working on a master's degree in business administration from the University of Texas—Dallas. His personal interests include looking for ways to improve products and processes, spending time with family, and, when time permits, squeezing in a round of golf.

Moody Dreiza is a senior product manager for stacked CSP at Amkor Technology Inc (Chandler, AZ). He previously spent more than four years in Amkor's design center supporting CSP and PGA design through design-tool automation. He has a bachelor's degree in mechanical engineering from the University of Manchester Institute of Science and Technology (Manchester, England). His personal interests include travel and mountain biking.

Obtain a lower dc voltage from a higher voltage power supply

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

You can use the circuit in **Figure 1** to obtain a low regulated voltage, such as 5V dc, from a higher voltage, rectified, sinusoidal voltage source without resorting to an electrically noisy dc/dc converter or wasting watts in a dropping resistor. This application requires a regulated 5V-dc source, but a transformer supplies 18V rms to a full-wave bridge rectifier. During the charging phase, two equal-value electrolytic capacitors, C_1 and C_2, receive charging current when connected in series through forward-biased diodes D_1 and D_2. An enhancement P-channel MOSFET transistor, Q_1, an International Rectifier (www.irf.com) IRF-9530, remains off because its gate receives a slightly positive reverse-gate-bias voltage due to zener diode D_4's forward-voltage drop. Each capacitor charges to approximately one-half the peak value of the rectified voltage minus the forward-voltage drops that D_1 and D_2 present. The full-wave bridge rectifier, D_5, or Graetz bridge, produces these drops (**Reference 1**).

When the discharge phase begins, D_1 gets reverse-biased, and capacitor C_2 discharges through the load that voltage regulator IC_1 presents. Subsequently, the anode voltage of diode D_1 continues to decrease, Q_1's gate-to-source voltage becomes negative, and the transistor conducts, allowing C_1 to discharge into the load through forward-biased diode D_3. In effect, the two capacitors charge in series and discharge in parallel into the load, halv-

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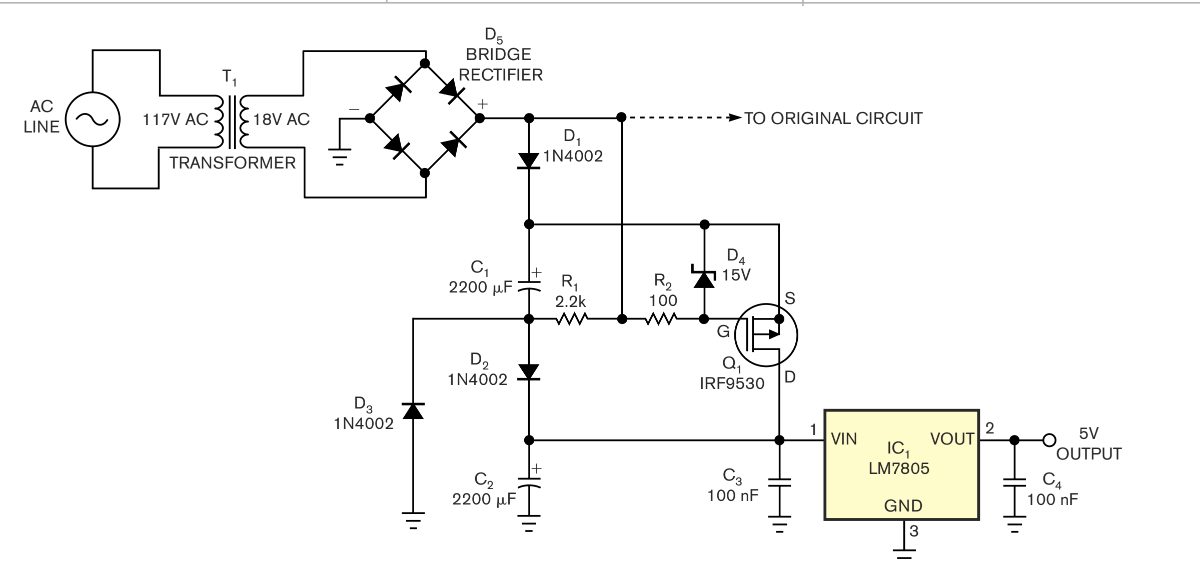

Figure 1 In this unconventional step-down circuit, capacitors C_1 and C_2 charge in series and discharge in parallel, reducing the voltage applied to regulator IC_1.

ing the raw rectified voltage and ripple voltage at IC_1's input. During C_1's discharge, zener diode D_4 protects Q_1 by clamping its gate-to-source voltage within its maximum rating.

To function properly, the circuit requires a minimum load current; the regulator's quiescent-current drain is usually enough. Otherwise, capacitor C_2 charges to the peak voltage available from D_5. The values of C_1 and C_2 and the ratings of the remaining components depend on the maximum load current required. The values of resistors R_1 and R_2 are not critical. Note that Q_1 functions as a switch; selecting a device with low on-resistance limits Q_1's power dissipation. EDN

REFERENCE

1 www.answers.com/topic/graetz-ag.

Line-powered driver lights up high-power LEDs

Aaron Lager, Masterwork Electronics, Rohnert Park, CA

Using LEDs has gained popularity as a method of saving power for general-purpose lighting, but an efficient method for driving them has also become a necessity. For example, Lumileds' (www.lumileds.com) Luxeon devices create lighting effects or room lighting. Providing power to a few LEDs may require only a current-limiting resistor, but illumination applications need a string of 20 or more LEDs to provide light over an area. Based on On Semiconductor's (www.onsemi.com) NCP1200A, a 100-kHz PWM current-mode controller for universal offline power supplies, the circuit in **Figure 1** provides a low-cost, offline constant-current source for powering multiple LEDs. Although designers typically configure it to provide a voltage source, in this application, the NCP1200A provides a constant-current source. **Figures 2** and **3** show close-ups of the circuit.

A full-wave bridge rectifier, D_2 to D_5, and filter capacitor C_1 provide approximately 160V dc to the conversion circuit, IC_1, and its associated components. Resistor R_3 alters the bias for IC_1's current-sense pin and, at 6.2 kΩ, allows the use of a 1.2Ω sense resistor for R_6. Decreasing R_6 not only reduces costs over a higher wattage sense resistor, but also improves the circuit's efficiency. Capacitor C_3 stabilizes the feedback network's current and carries a 400V rating in case of an open circuit in the LED string. An RC network comprising R_5 and C_4 provides a small amount of lowpass filtering to the CS pin.

Bleeder resistors R_1 and R_2 eliminate any shock hazard across the ac-line plug's prongs when you disconnect it. Although you can use a 1-MΩ through-hole-mounted resistor, two surface-mounted 500-kΩ series resistors cost less and provide the required track-

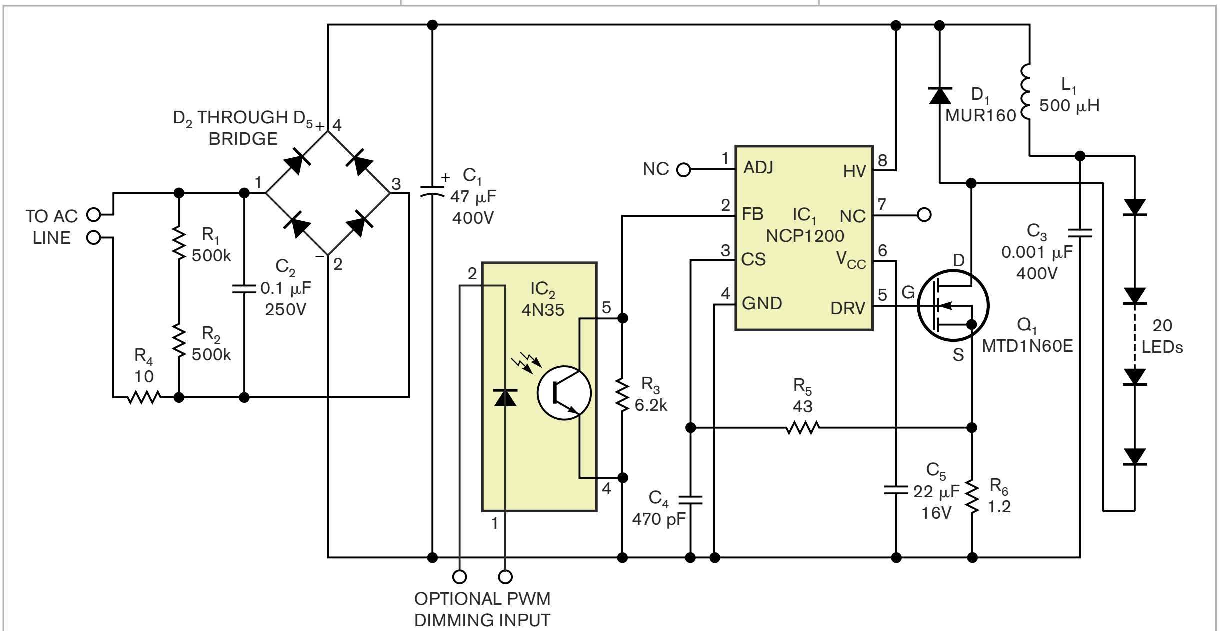

Figure 1 An offline constant-current source drives a string of high-output LEDs.

to-track pc-board spacing for line-voltage applications. Use a capacitor rated for line-bypass service for capacitor C_2. You can use any power MOSFET with a suitable breakdown voltage and a low on-resistance, such as an MTD1N60E or IRF820, for Q_1. Inductor L_1, a 500-μH device, should be able to operate at 100 kHz and handle more than 350 mA of continuous current. You can use an inductor from Coilcraft's (www.coilcraft.com) RFB1010 or DR0810 series of surface-mount inductors, or you can experiment with inductors manually wound on suitable core materials. As an option, adding optoisolator IC_2 allows microcomputer-controlled illumination dimming using pulse-width modulation of IC_1's feedback terminal, Pin 2.

To understand the economic motivation for using LEDs as illuminators, compare the light output of a string of 20 1W, white Luxeon emitters with a standard incandescent light bulb. Each LED provides 45 lumens, or 900 lumens for a string of 20 LEDs. The average forward voltage per LED is 3.42V for a power dissipation of 1.197W each at a forward current of 350 mA. Thus, the 20-LED string dissipates 23.94W. Factoring in a conservative 80% efficiency for the power supply, the power the system consumes becomes 28.73W for a light-emission-efficiency value of 900 lumens/29W or 31 lumens/W. The Luxeon emitters also carry a rating for 100,000 hours, or approximately 11 years, of operation.

In contrast, a standard 60W Philips incandescent light bulb produces 860 lumens for 1000 hours, or just over a month, at an efficiency of only 14 lumens/W. From a power-consumption viewpoint, the LED-based design is twice as efficient as the incandescent-bulb-based design and thus reduces power consumption and cost. In addition, the LED design imposes no additional maintenance costs for replacement bulbs and labor. EDN

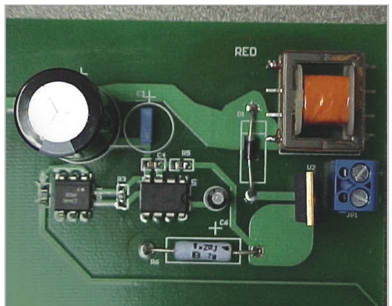

Figure 2 A close-up view of the circuit of Figure 1 shows inductor L_1 in the upper right corner.

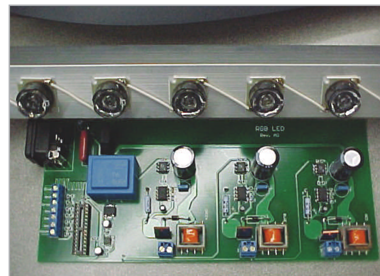
Figure 3 This version of the circuit comprises three constant-current driver channels. An LED light-bar assembly is above the pc board.

Rectifier tracks positive and negative peaks

Harry Bissell Jr, Welding Technology Corp, Farmington Hills, MI

Signals ranging from music to complex control-system waveforms may contain unequal positive and negative peak amplitudes. An "envelope-follower" circuit can track unequal peaks, but the ability to select a desired peak can enhance the circuit's performance (**Reference 1**). The circuit in **Figure 1** applies a new twist to a classic absolute-value circuit. Applying an input signal to R_1 (full) produces an output equal to the input's absolute value. Applying an input signal to R_6 (positive) or R_7 (negative) produces outputs of positive or negative half-cycles, respectively. **Figure 2** illustrates all three modes of operation.

Understanding the circuit is simple if you consider that op amp IC_{1A} strives to maintain its inverting input at virtual ground. For example, applying −1V to the negative input, R_7, drives the anode of D_1 to −333 mV. IC_{1A}'s output, Pin 1, drives D_2's cathode positive enough to force D_2's anode voltage to 333 mV. Because IC_{1A}'s inputs now rest at 0V, D_1 is effectively reverse-biased and out of the circuit. The 333 mV available at D_2's cathode also applies to IC_{1B}'s noninverting input, Pin 5, and IC_{1B} must balance its input voltages by driving its output, Pin 7, to 1V. IC_{1B}'s inverting input, Pin 6, goes to 333 mV. The voltage drop across R_4 thus equals 666 mV. One-third of the input current flows through the series connection of R_2 and R_3, and two-thirds flows in R_4. To achieve unity gain, R_7's value equals that of R_2+R_3 in parallel with R_4.

Applying a positive input to R_7 causes IC_{1A}'s output to go negative by a voltage equal to one forward-diode drop and thus holds D_1's anode at ground. D_2 is reverse-biased, and both of IC_{1B}'s inputs rest at 0V. The circuit's output is thus 0V. Applying an input voltage at R_6 yields similar operation. A positive input causes an equal-value positive output, and a negative input produces a 0V output. You can ignore the effects of IC_{1B}'s high input impedance, which are negligible. To maintain unity gain, the value of R_6 is twice that of R_3.

Resistors R_1, R_2, R_3, R_4, and R_5 are of equal value and close tolerance. Note that IC_1's power-supply connections require bypass capacitors (not shown). To minimize errors, use a low-impedance source or buffer amplifier to drive the circuit. You can use a three-posi-

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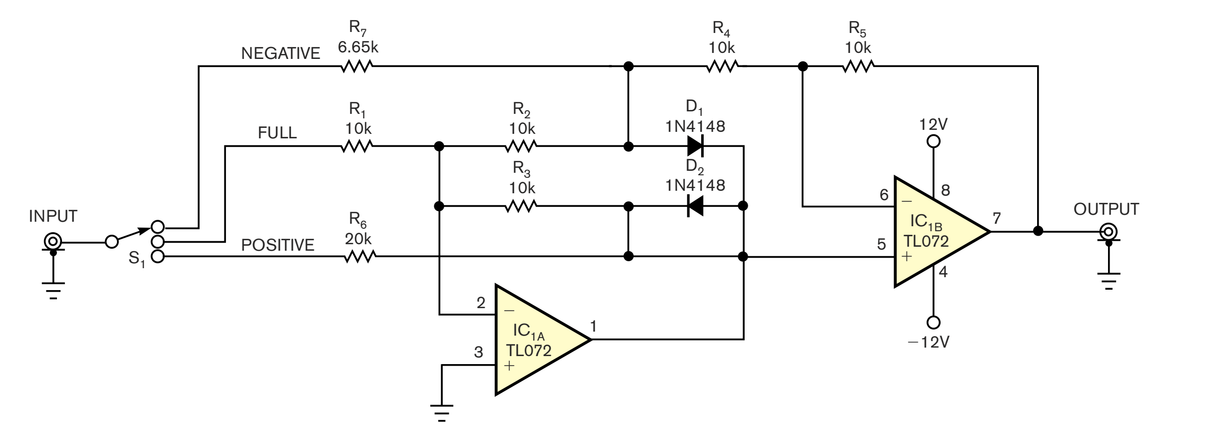

Figure 1 Use this versatile precision rectifier circuit to recover a signal's positive peaks, negative peaks, or both in full-wave mode.

tion rotary switch for input-mode selection, or an on/on/on toggle switch, such as C&K Components' 7211, available from Digi-Key Corp (www.digikey.com) and other sources, or a similar switch, wired as a three-way selector. (See the manufacturer's data sheet for a connection diagram.) You can also use separate connectors for the inputs, but connect no more than one input at a time. EDN

REFERENCE

1. Bissell, Harry, "Envelope follower combines fast response, low ripple," *EDN*, Dec 26, 2002, pg 59, www.edn.com/article/CA265499.

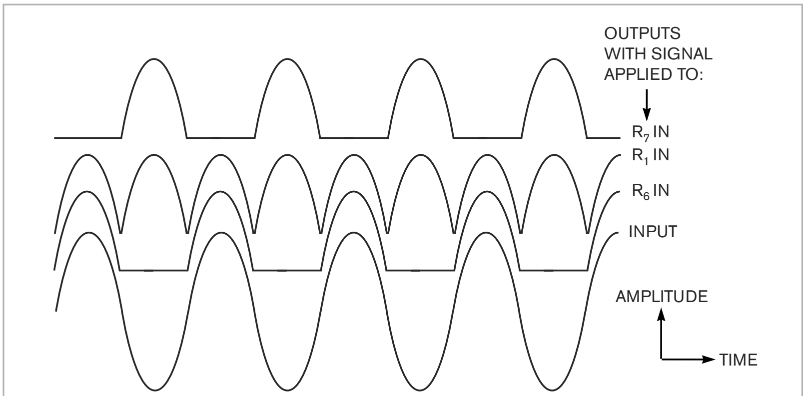

Figure 2 This waveform plot shows the circuit's outputs for a sine-wave input connected to the negative, full, and positive inputs, respectively. Traces are vertically offset for clarity.

Isolated indicator signals telephone line's status

Yongping Xia, Navcom Technology, Torrance, CA

Part 68 of the FCC's (Federal Communications Commission, www.fcc.gov) telecommunications regulations requires that certain signaling equipment connecting directly to the public-telephone network must present a line-to-line resistance of at least 5 MΩ. In addition, status signals that equipment derives from the phone lines must include electrical isolation to prevent interaction between earth grounds from the telephone network and attached control or communications equipment. Although a transformer can provide isolation for voice-frequency signals, the telephone-line-status-indicator circuit in **Figure 1** meets FCC isolation requirements without incorporating a transformer (**Reference 1**). A diode bridge, D_1 through D_4, and R_1, a 5.6-MΩ resistor, supply a small amount of dc power from the phone line to a nanopowered combination comparator and a 1.2V voltage reference, IC_1. The Maxim (www.maxim-ic.com) MAX917 IC draws only 0.75 μA at $1.8V_{CC}$.

Resistors R_2 and R_3 form the detection-voltage divider, and R_4 provides hysteresis. When IC_1's output goes low, R_4 and R_3 form a parallel combination of 3.26-MΩ resistance. To reach the comparator's reference voltage of 1.245V, the voltage across C_1 must reach at least 5.06V. Once IC_1's output

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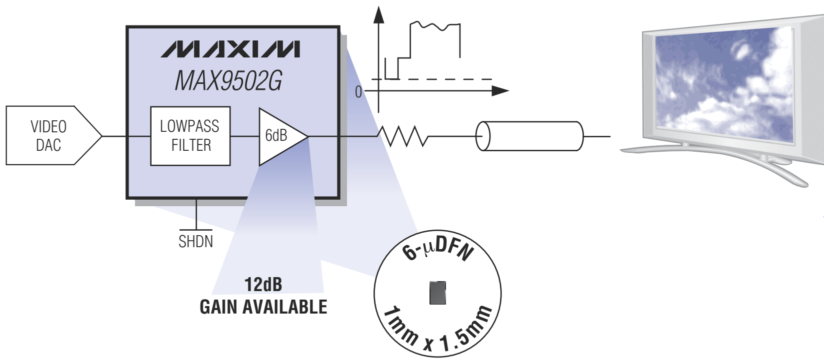

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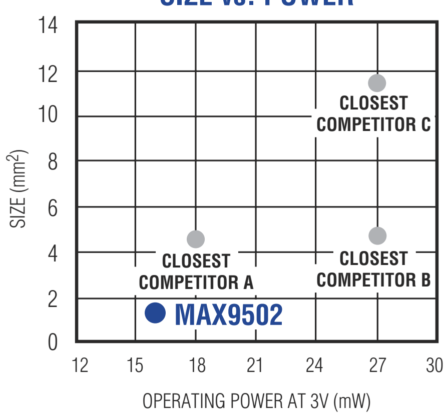
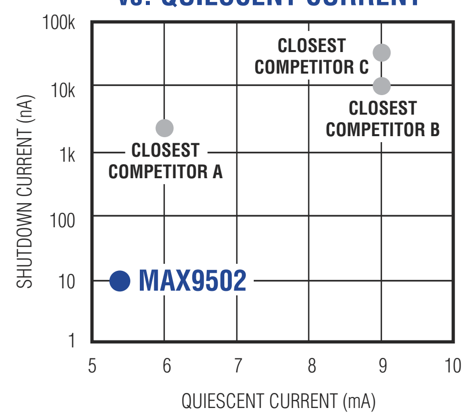


SHUTDOWN CURRENT vs. QUIESCENT CURRENT



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goes high, R_4 and R_2 form a parallel resistance of 6.67 MΩ, and the voltage across C_1 must reach 3.37V to deliver a 1.245V input to the comparator. IC_1's output drives a photocoupler, IC_2, a Toshiba (www.semicon.toshiba.co.jp) TLP190B. Unlike other photocouplers, IC_2 includes an array of photodiodes that, when illuminated, delivers a voltage output. Although weak by power-conversion standards, the photocoupler's output can deliver several microamperes at an open-circuit voltage that exceeds 7V, or enough to drive a MOSFET's gate or a microprocessor's input pin. In addition, the TLP190B carries a 2500V-rms emitter-to-detector isolation-voltage rating.

When a telephone is not in use, the on-hook voltage across its line of approximately −48V produces a current of 7 to 8 μA through R_1, which imposes a low-leakage requirement on C_1. The prototype version of the circuit uses an X5R-characteristic ceramic capacitor. When the voltage across C_1 exceeds 5.06V, IC_1's output goes high and drives IC_2 through R_5, discharging C_1. When the voltage across C_1 decreases to 3.37V, IC_1's output goes low, and C_1 recharges. The output from IC_2 comprises a 1.4-msec-wide voltage pulse with a repetition period of approximately 240 msec. When the phone is off the hook, the voltage across its lines drops to a few volts, which don't sustain pulse generation. EDN

REFERENCE

1. www.fcc.gov/wcb/iatd/part_68.html.

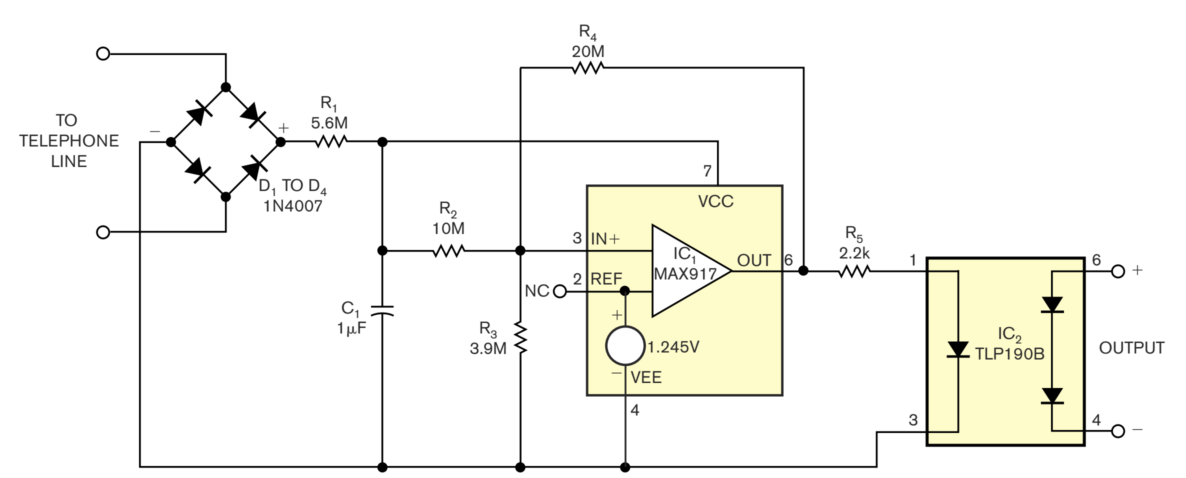

Figure 1 Drawing minuscule amounts of power from a telephone line, this isolated-output circuit indicates whether the line is in use.

Circuit converts DAC's outputs from single-ended to differential mode

Liam Riordan, Analog Devices, Limerick, Ireland

High-speed DACs, such as Analog Devices' AD9776/78/79 TxDAC family, offer differential outputs, but, for low-end ac applications or high-precision level-setting applications, a single-ended current-output DAC with a differential-conversion circuit provides a novel approach to generating differential-waveform-control functions. The basic circuit in **Figure 1** combines a current-output DAC, IC_1, such as the 8-bit AD5424 DAC, with a single-ended-to-differential op-amp stage—IC_2, IC_{3A}, and IC_{3B}—to generate the desired outputs. For dual-power-supply applications, you select the DAC's unipolar mode of operation to achieve optimum performance from the DAC. Using a single op amp, the DAC provides two-quadrant multiplication or a unipolar output-voltage swing. The DAC's output requires a buffer because changing the code applied to the DAC's input varies its output impedance.

This equation defines the circuit's output voltage: $V_{OUT} = -V_{REF} \times (D/2^N)$, where N defines the number of input bits, V_{REF} is the reference voltage, and D is the decimal equivalent of the binary code. To generate a positive common-mode voltage, you use a negative voltage for the DAC's reference voltage. The DAC's internal design accommodates ac reference input signals of −10 to +10V. In this mode, the DAC provides a 5M-sample/sec maximum update rate for one-quarter full-scale code changes when you operate it from a 5V power supply. Use resistors R_1 and R_2 only if your application requires adjustable gain.

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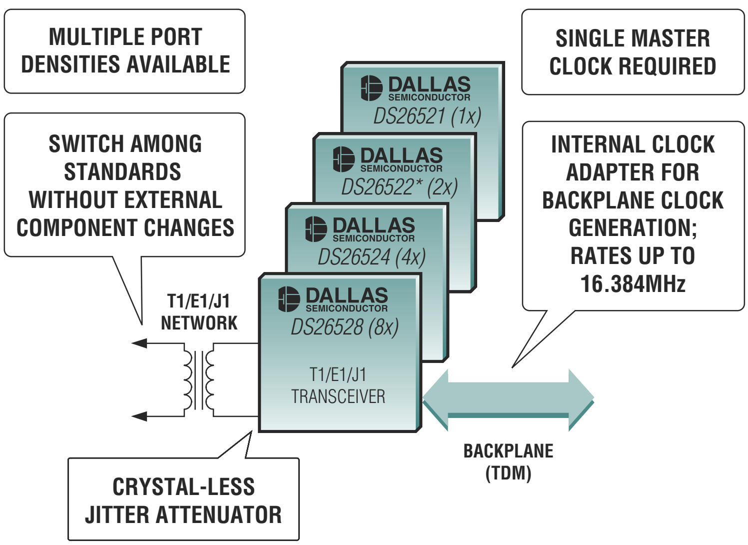

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The single-ended-to-differential stage comprises two cross-coupled op amps, which resistors R_5 and R_6 configure as a unity-gain follower. To yield a symmetric circuit, the outputs also drive each other as unity-gain inverters through R_7 and R_8. The voltage you apply to the positive terminal of op amp IC_2 sets the circuit's common-mode voltage. Resistors R_3 and R_4 control the amplitude of the differential voltage. Review your application's output-load requirements and the op amps' input- and output-voltage capabilities.

For single-supply applications, you can use a current-output DAC in reverse mode, in which you apply the reference voltage, V_{IN}, to the DAC's I_{OUT1} pin and take the output voltage from the DAC's V_{REF} terminal (**Figure 2**). In this configuration, a positive reference voltage produces a positive output voltage. This circuit does not use the DAC's feedback resistor, R_{FB}, and its connection to I_{OUT1} prevents stray capacitance effects. The DAC's reference input "sees" an impedance that varies with the applied code and thus requires a low-impedance source.

Note that the switches in the DAC ladder no longer have the same source-to-drain drive voltage, which in turn limits the input voltage to low voltages. As a result, the switches' on-resistances differ and degrade the DAC's linearity. Also, this mode limits the max-

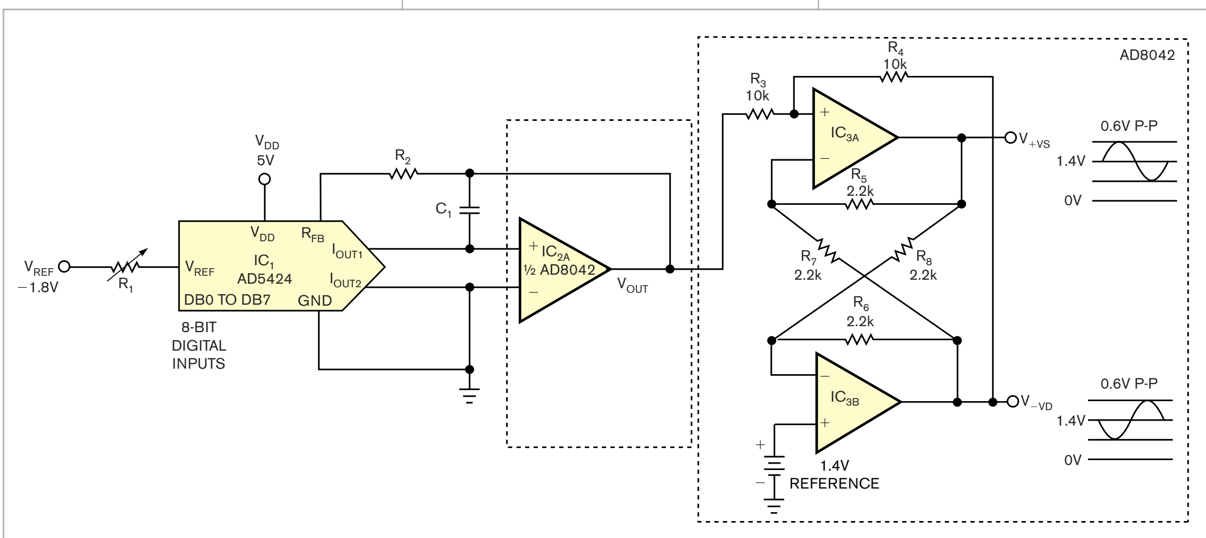

Figure 1 This basic circuit combines a current-output DAC, IC_1, with a single-ended-to-differential op-amp stage–IC_2, IC_{3A}, and IC_{3B}–to generate the desired outputs.

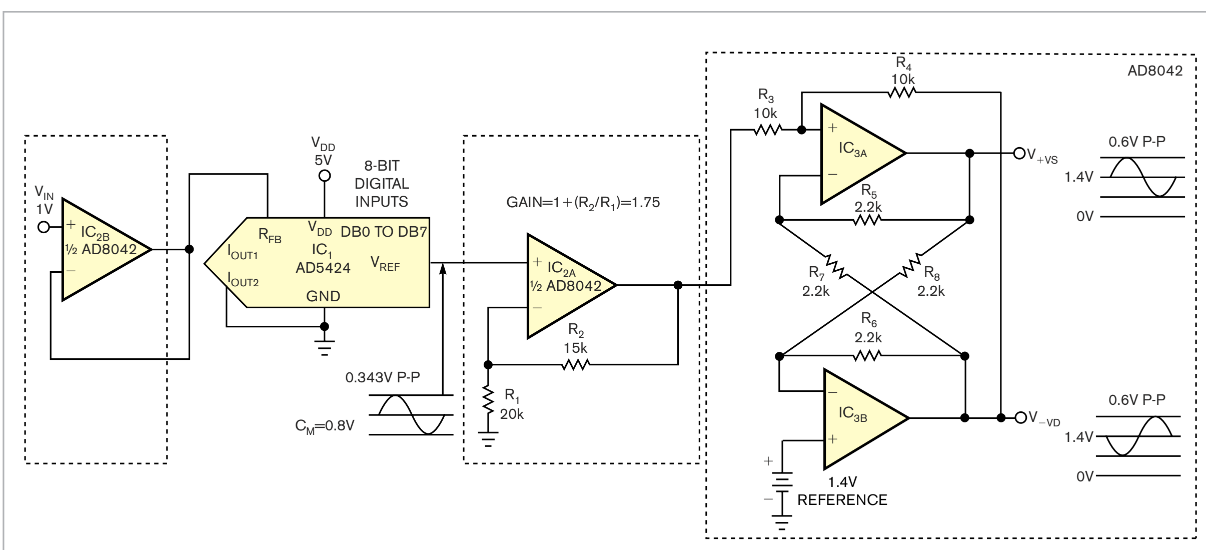

Figure 2 In this configuration, a positive reference voltage produces a positive output voltage.

LINEAR TECHNOLOGY

DESIGN NOTES

Tiny Monolithic Step-Down Regulators Operate with Wide Input Range – Design Note 390

Kevin Huang

Introduction

Automotive batteries, industrial power supplies, distributed supplies and wall transformers are all sources of wide-ranging high voltage inputs. The easiest way to step down these sources is with a high voltage monolithic step-down regulator that can directly accept a wide input range and produce a well-regulated output. The LT®3493 accepts inputs from 3.6V to 36V and LT3481 accepts inputs from 3.6V to 34V. Both provide excellent line and load regulation and dynamic response. The LT3481 offers a high efficiency solution over a wide load range and keeps the output ripple low during Burst Mode® operation while the LT3493 provides a tiny solution with minimal external components. The LT3493 operates at 750kHz and the LT3481 has adjustable frequency from 300kHz to 2.8MHz. High frequency operation enables the use of small, low cost inductors and ceramic capacitors.

Low Ripple and High Efficiency Solution over Wide Load Range

The LT3481 is available in a 10-pin MSOP or a 3mm × 3mm DFN package with an integrated 3.8A power switch and external compensation for design flexibility. The switching frequency can be programmed from 300kHz to 2.8MHz by using a resistor tied from the RT pin to ground. Figure 1 shows the LT3481 producing 3.3V at 2A from an input of 4.5V to 34V. Figure 2 shows the circuit efficiency at 12V input.

The LT3481 offers low ripple Burst Mode operation that maintains high efficiency at light load while keeping the output voltage ripple below $15mV_{P-P}$. During Burst Mode operation, the LT3481 delivers single cycle bursts of current to the output capacitor followed by sleep periods when the output power is delivered to the load by the output capacitor. Between bursts, all circuitry associated with controlling the output switch is shut down reducing the input supply current to 50µA. Figure 3 shows the inductor current and output voltage ripple under single pulse Burst Mode operation from 12V input to 3.3V output. As the load current decreases to a no load condition, the percentage of time that the LT3481 operates in sleep mode increases and the average input current is greatly reduced resulting in high efficiency. The LT3481 has a very low shutdown current (less than 1µA) which significantly extends battery life in applications that spend long periods of time in sleep or shutdown mode.

The high side bootstrapping boost diode is integrated into the IC to minimize solution size and cost. When the output voltage is at least 2.8V, the anode of the boost diode can be connected to output. For output voltages lower than 2.5V, the boost diode can be tied to the input. For systems that rely on a well-regulated power source, the LT3481 provides a power good flag that signals when V_{OUT} reaches 90% of the programmed output voltage. A

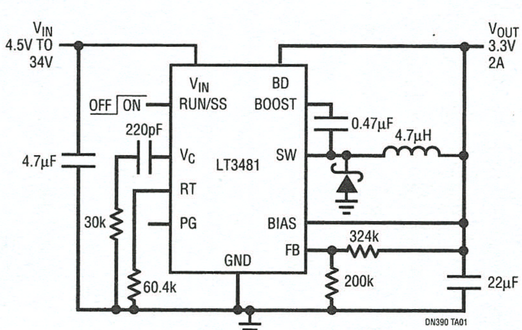

Figure 1. 800kHz LT3481 DC/DC Converter Delivers 2A at 3.3V Output

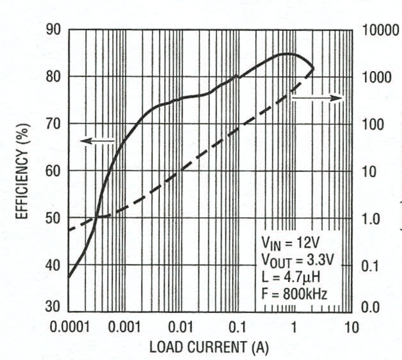

Figure 2. Efficiency vs Load Current for Figure 1 Circuit

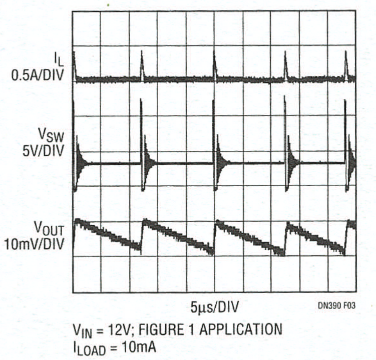

Figure 3. LT3481 Burst Mode Operation at 10mA Load Current

resistor and capacitor on the RUN/SS pin programs the LT3481's soft-start, reducing maximum inrush current during start-up. Figure 4 shows the circuit and start-up waveform.

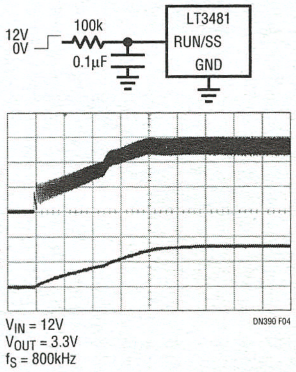

Figure 4. Soft-Start of the LT3481

Small Solution Size

The LT3493 includes an internal 1.75A power switch in a tiny 6-pin DFN package (2mm × 3mm). The current mode control circuit with its internal loop compensation eliminates external compensation components, minimizing component count and reducing the PC board space to less than 50mm^2. The LT3493's reference voltage is 0.78V, making it suitable for applications with low output voltage. Figure 5 shows an application of the LT3493 switching at 750kHz. This circuit generates 3.3V from an input of 4.2V to 36V. In applications where the circuit is plugged into a live input source through long leads, a high

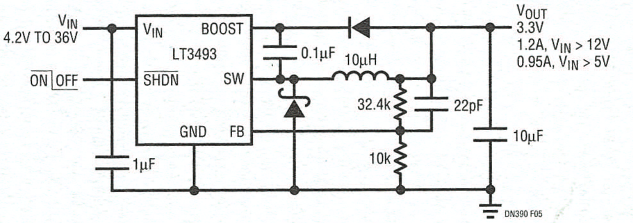

Figure 5. LT3493 Wide Input Range DC/DC Converter Application to 3.3V

ESR electrolytic capacitor at the input is recommended to damp the overshoot voltage. Refer to AN88 for details. The $\overline{SHDN}$ pin can be driven through an external RC filter to soft-start the LT3493.

Additional Features of LT3481 and LT3493

During short circuit, both parts offer cycle-by-cycle current limit and frequency foldback which decreases the switching frequency when the output is low. The low frequency allows the inductor current to safely discharge.

Conclusion

The wide input ranges, small size and robust design of the LT3493 and LT3481 make them an excellent choice for a wide variety of step-down applications. Their high input voltage, high power switch capability and excellent package thermal conductivity add to their versatility.

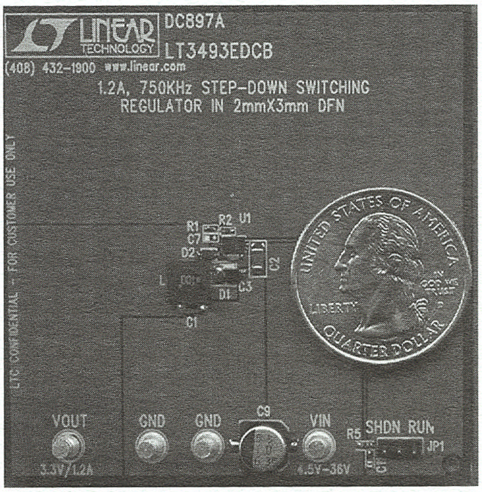

Figure 6. LT3493 Demo Board

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imum update rate to 1.5M samples/sec. You can use sections of a dual op amp to buffer the DAC's input and to amplify the DAC's output voltage (**Figure 3**). The circuit's intended application determines your choice of supporting amplifiers. For lower speed, precision applications, the op amp requires low input-bias currents and low input-offset voltage to avoid degradation of the DAC's DNL (differential-nonlinearity) performance. For example, the AD8628 offers 100-pA maximum bias current at room temperature and 5-μV maximum input-offset voltage. The op amp's low-frequency noise is important in precision level-setting applications, and the AD8628 specifies 0.1- to 10-Hz noise of less than 0.5 μV p-p. Its rail-to-rail inputs and outputs make it ideal for use in single-supply circuits.

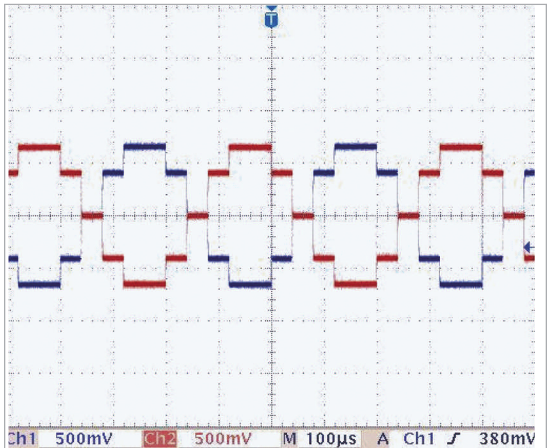

Figure 3 The single-ended-to-differential conversion of a digitized, eight-point sine wave produces differential outputs.

For high-speed-system applications, the op amp's slew rate must not dominate the DAC's slew rate. The op amp's bandwidth must be large enough to drive the feedback load and must not limit the circuit's overall bandwidth, and the DAC's output- voltage settling time should determine the circuit's maximum update rate. The AD8042 in **figures 1** and **2** offers 170-MHz bandwidth and a 225V/μsec slew rate, allowing it to easily achieve these results. Other high-speed op amps, such as the AD8022, AD8023, and AD8066, also work well in this application.

The DAC consumes only 0.4 μA of power-supply current, and the op amps thus dominate the circuit's power consumption. To minimize the area for the circuit on a pc board, you can replace all four op amps in **Figure 2** with a single AD8044 quad op amp. The single-ended-to-differential conversion of a digitized, eight-point sine wave in the presence of a 1.4V common-mode voltage and a 0.6V differential signal produces differential outputs (**Figure 3**).EDN

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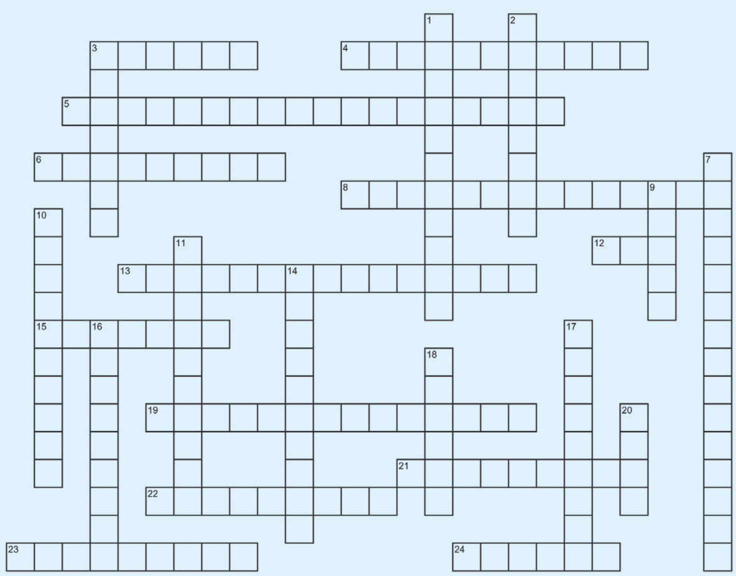

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DOWN

1 System with both analog and digital waveforms
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3 External stimulus that initiates instrument functions
7 Technique used to ensure instrument clocking occurs at the same time
9 Unwanted signals
10 The smallest amount of input signal change that an instrument or sensor can detect.
11 Next generation, high-bandwidth, high speed PC bus based on PCI
14 Frequency at which the ADC converts analog to digital data
16 -3dB below the passband frequency
17 Needs to be matched
18 Annual conference of virtual instrumentation held in Austin, TX
20 Low Voltage Differential Sampling

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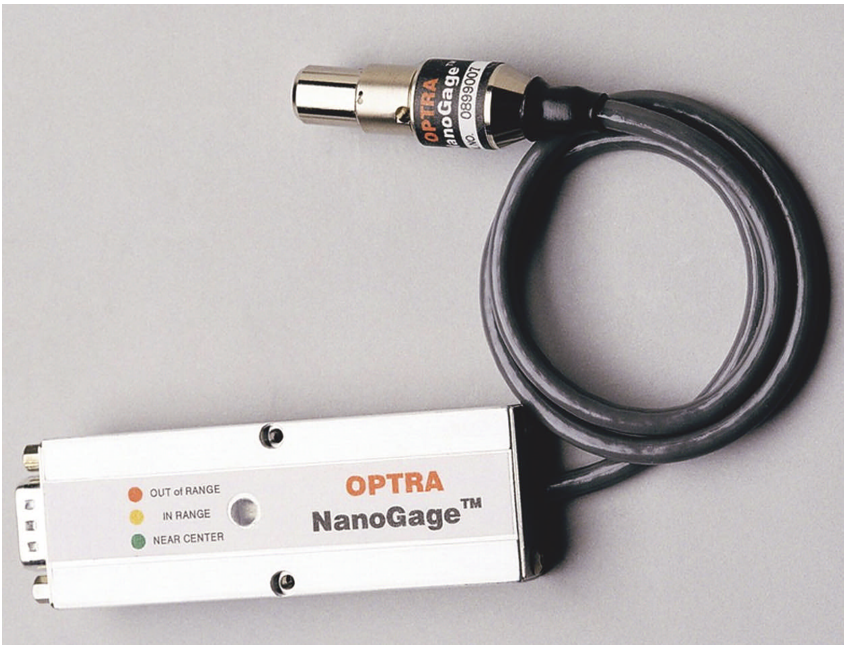


Short-range position sensor provides large measurement bandwidth

Measuring 0.5-in. in diameter and 2.2 in. in length, the NanoGage Model 100 short-range position sensor has an aluminum structural body. Features include a 100-micron linear-measurement range, a ±400-micron signal-capture range, and a 15-nm-rms measurement bandwidth at 100 kHz. The device suits a range of applications, including automated focusing at a specific surface height; run-out measurements, maintaining a closed-loop position; or vibration measurements. The NanoGage costs $2995.

Optra Inc, www.optra.com

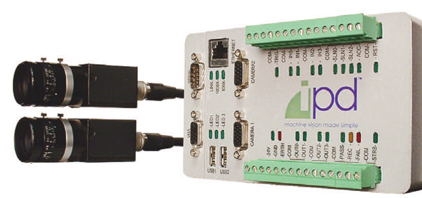
Dual-axis servo amplifier can drive two independent motors

The Model 800-1514 dual-axis servo amplifier for current and torque control of brushless servo motors accepts encoder- and Hall-feedback data from a range of servo-motor types, including Yaskawa Sigma-Mini and Panasonic Minas-A motors. Controlling drive torque with a ±10V command from a motion controller or programmable-logic controller, the device features a standard buffered encoder output and optically isolated control signals. Using CME 2 Windows software, the device communicates with the setup computer by an RS-232 link. Peripherals include operation at 20 to 55V with an isolated dc supply; two independently controlled, 4A-peak, 3A-continuous outputs aiming at driving high-performance, three-phase motors; and a 5V-dc-output amplifier. Targeting multiaxis equipment for semiconductor fabrication, test and measurement, and automated assembly, the Model 800-1514 costs $690.

Copley Controls, www.copleycontrols.com

Vision appliance supports one or two cameras

Adding on to the vendor's line of machine-vision appliances, the VA20 supports one or two cameras with the choice of sensor resolutions. Available in two versions, the VA20 includes the vendor's iNspect software, and the VA21 version also includes the Sherlock machine-vision software. The device has



the "smarts" inside the camera controller instead of on the camera head, allowing positioning alongside other automation controllers for easier interfacing. This feature also allows for easy mounting. Supporting 640×480 and 1024×768 sensor resolutions, a 1600×1200 higher resolution is also possible. The VA20 comes in a compact DIN-mountable enclosure and costs $3495.

DALSA Coreco Group, www.goipd.com

Sensorless-control platform targets energy-saving motors

Aiming at direct-drive, PMSM (permanent-magnet-synchronous-motor) washing machines, the IRMCS-3041 sensorless-control platform features an embedded FOC (field-oriented-control) algorithm for high-dynamic torque control, saving as much as 70% of energy usage. This addition to the iMotion fam-

ily also includes the IRMCF341 mixed-signal controller, companion intelligent power modules, development software, and design tools. The IRMCF341 washer-control IC integrates control- and analog-interface functions for sensorless-speed control of the PMSM or using dc-link-current measurements. Analog functions of the IC include a differential amplifier, dual sample-and-hold circuits, and a 12-bit ADC for sampling low-voltage signals over the dc-link shunt. Integrating a 60-MIPS, 8-bit 8051 microcontroller allows the application-layer software development to operate almost independently of the MCE (motion-control engine) without competing for system resources, such as interrupts or internal registers. The IRMCS3041 iMotion washer-platform reference design costs $995.
International Rectifier, **www.irf.com**

MICROPROCESSORS

Debugger supports ARM9 coprocessor

Featuring an unlimited number of breakpoints, the HiTop Version 5.20 debugger fully supports ARM9 coprocessors. The Exception Capture and Solution Assistant allows the localization of sources of exceptions. Free evaluation versions of HiTop Version 5.20 are available for downloading from the vendor's Web site.
Hitex Development Tools, **www.hitex.com**

Graphics-tool suite provides visualization

Enabling system visualization, the AxisView integrated graphics-tools suite comprises the HardwareView, ApplicationView, EventView, ProcessView, and DebugView tools. HardwareView builds a graphical representation of the multiprocessor subsystem and displays information about the system configuration. ApplicationView provides a graphical representation of the application, autogenerating AxisFlow configuration code and developing a template for the initialization of the application. The EventView true-multiprocessor-event analyzer allows event traces and ensures accurate time alignment. ProcessView supplies dynamic information on the CPU and memory usage at the application-task level and provides information on the system data flow. The DebugView multiprocessor-debugging tool features coordinated and grouped breakpoints. The suite also features the AxisFlow interprocessor-communications element, which supplies reconfigurable interconnections, and the AxisLib high-performance digital-signal-processing libraries, which support algorithms for the PowerPC AltiVec architecture.
Radstone Embedded Computing, **www.radstone.com**

Platform allows evaluation of FRAM devices

Supporting the VRS51L2070, the VersaKit-20xx evaluation platform comprises a set of probe vias and header footprints, an RS-232 transceiver, two DB9 connectors for UART access, and eight user LEDs. The device also includes two switches for manual reset/interrupt triggering, prototyping space, and JTAG access for in-circuit programming and real-time debugging of the VRS51L2070. An FM31256 processor companion, an FM25CL64 serial SPI FRAM (ferroelectric RAM), and an FM24CL64 serial I²C FRAM on the board allow evaluation of the vendor's FRAM devices. The VersaKit-20 costs $99, including a development board, the Versa-JTAG programming/debugging interface, a DB25 parallel cable, and a power supply.

Ramtron International, www.ramtron.com

Packet-processor family supports tunneling

Supporting tunneling capabilities, the Prestera 98DX2x5 packet-processor family provides multilayer and 10-Gbit Ethernet. Using MPLS-based VPWS (virtual-private-wire-service) and VRF (virtual-routing-and-forwarding) functions allows the device to deliver application-aware secure service through Layer 2 and Layer 3 VPNs (virtual private networks). Features include 24-Gbit ports, four 10-Gbit XG ports, an on-chip buffer memory, and an integrated TCAM (ternary content-addressable memory). Additional features include line-rate L2 bridging, L3 versions 4 and 6 routing, comprehensive Internet Protocol-multicast support, advanced L2- and L4-traffic classification, filtering, and prioritization.

Marvell, www.marvell.com

DSP family adds core with fewer gates

Having fewer gates than the vendor's other family members, the new Ceva-X1622 DSP core provides backward code compatibility with the Ceva-X1620 DSP. This fully synthesizable DSP features an enhanced memory architecture, including a 64- or 128-kbyte configurable memory and configurable two- or four-block memory-bank organizations. Features include a 16-bit, fixed-point dual-MAC (multiply-accumulate) VLIW (very-long-instruction-word) architecture combined with SIMD (single-instruction-multiple-data)-multimedia operation, built-in multimedia instructions, eight instructions executed in parallel, 16- or 32-bit variable instruction widths, and 4 Gbytes of byte-addressable-memory space.

Ceva Inc, www.ceva-dsp.com

Starter kit comes with STR912F microcontroller

Targeting STMicroelectronics' STR912F controller, the vendor's starter kit contains an evaluation board with the controller and a USB-based Tantino for ARM7 to ARM9 JTAG debugging. Additional features include a quick-start guide, a 96 MHz internal clock, and a CD with the HiTop development environment. The environment includes examples, a GNU complier, a HiSIM ARM instruction-set simulator, and the Tessy software-test tool. The evaluation software comes in a 16-kbyte limited code size, but users can upgrade it to an unlimited version.

Hitex Development Tools, www.hitex.com

Processor family adds devices with flash memory

Adding to the Blackfin family, the 400-MHz ADSP-BF539 and ADSP-539F processors run at automotive temperatures and support Green Hills Software's Integrity real-time operating system. Two other new family members, the 500-MHz ADSP-BF538 and ADSP-538F processors, combine CAN (controller-area-network), serial-port-UART, SPI, two-way, and general-purpose-I/O interfaces with dual DMA controllers. The first Blackfin processors using flash memory, the ADSP-539F and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MICROPROCESSORS

-538F incorporate either 512 kbytes or 1 Mbyte of flash.
Analog Devices, www.analog.com

Upgrade adds floating-point support and a C2H compiler

Version 6.0 of the Nios II EDS (embedded-design-suite) processor includes 32-bit, single-precision, IEEE 754-compatible floating-point support and the Nios II C2H (C-to-hardware-acceleration) compiler. It is available as a set of Nios II custom instructions. Active subscribers automatically receive the Version 6.0 upgrades for Nios II processors and Nios II EDS and have access to a free evaluation license for the Nios II C2H compiler. Annual Nios II subscriptions cost $495, and the Nios II C2H compiler, available as an integrated plug-in to the Nios II IDE, costs $2995 per seat.
Altera, www.altera.com

EDA TOOLS

Simulator aims at RF and microwave-circuit designs

Targeting RF and microwave-circuit designers, the EMDS (Electromagnetic Design System) allows users to simulate and analyze electromagnetic effects for greater insight into their design's performance. The device provides information that allows designers to make adjustments before they start physical prototyping, reducing design iterations. This initial release of the system provides basic design-flow integration with the vendor's ADS (Advanced Design System), allowing users to bring layout designs from ADS into EMDS for 3-D analysis. Upgrades for the system include increasing levels of integration with ADS and the company's Genesys environment. The EMDS 2006A costs $15,000.
Agilent Technologies, www.agilent.com

Part-list-management tool adds to pc-board tool set

Joining the Cadstar pc-board tool set, the Starturn part-list-management tool improves the post-design documentation process by exporting functions for BOMs (bills of materials) in HTML, Microsoft Excel, and XML formats with the ability to specify which design fields to include. The Cadstar drill-drawing function generates drill tables within the pc-board design and improves the markup feature. Drill-drawing exports and report generation allow users to cite circuit references in multiple places within the design. A new "where-used" search capability monitors part obsolescence.
Zuken, www.zuken.com

IP library targets machine-vision applications

Running on an FPOA (field-programmable-object-array) chip, the vendor's new machine-vision IP (intellectual-property) library contains a color-space-conversion core and a flat-field-error-correction core. The color-space-conversion core supports a 1 billion/sec incoming-pixel rate, and the flat-field-error-correction core supports a 500 million/sec incoming-pixel rate. A 500 million-pixel/sec rate corresponds to a 2000×2000-resolution image sensor at 125 frames/sec.
MathStar, www.mathstar.com

COMPUTERS & PERIPHERALS

500-Gbyte hard drive supports a 1.2 million-hour MTBF

Available in a 500-Gbyte capacity, the enterprise-class WD RE2 (RAID Edition) SATA hard drive features a 3-Gbps data-transfer rate. The device includes 1.2 million hours MTBF at a 100% duty cycle. Additional features include an NCQ (native-command-queuing) feature, a 16-Mbyte cache, and a five-year limited warranty. Targeting network-attached storage, direct-attached server storage, and video-surveillance environments, the RE2 SATA hard drive costs $349.99.

Western Digital Corp, www.westerndigital.com

JBOD products include adapters, port multipliers, and USB 2.0 controllers

Allowing users to build a multiterabyte external-storage device, this new JBOD (just-a-bunch-of-disks)-product family features a USB 2.0 controller, an eSATA port multiplier plus RAID5 (redundant-array-of-inexpensive-disks) controller, and a dual-port IDE-to-SCSI adapter. The JBOD USB 2.0 adapter supports four 2.5-in. IDE hard drives through a high-speed USB 2.0 connection and is compatible with Windows XP, 2000, and 2003. Combining as many as five SATA hard drives into one eSATA connection, the 5X1 eSATA port multiplier has a RAID 5, RAID 0, RAID 1, no-RAID, or JBOD configuration. Attaching two IDE hard drives to a SCSI bus, the dual-port adapter enables the two IDE devices to function transparently as SCSI using a single SCSI ID. The drives can operate as individual drives or as a large combined drive using the JBOD feature. The SCSI also supports a 160 Mbps maximum data transfer. The USB 2.0 adapter, the eSATA-port multiplier, and the dual-port adapter cost $59, $89, and $109, respectively.

Addonics, www.addonics.com

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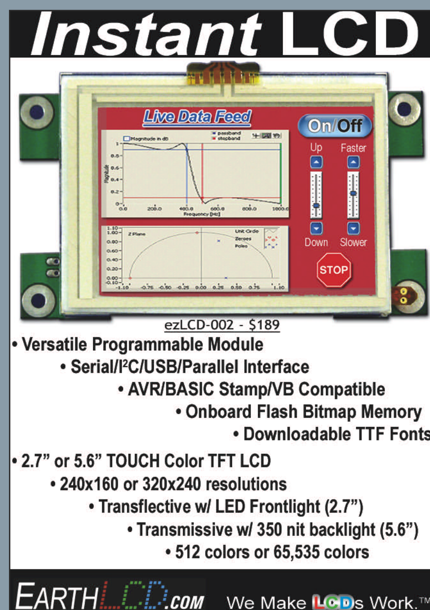

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STATS | Operating altitude: as high as 70,000 ft / Commercial deployments: zero

Broadband from airships: a lot of hot air?

In the late 1990s and early 2000s, anticipated demand for Internet access ran so high that several companies sprang up with plans to launch high-flying airships that would blanket cities with wireless coverage. The reasoning was that, hovering at 60,000 ft or higher, flying machines could serve an entire metro area at lower cost than a satellite launch or new wired infrastructure.

Angel Technologies (www.angeltechnologies.com) planned to use piloted, fixed-wing aircraft, which Scaled Composites (www.scaled.com) built. (Scaled Composites later became famous for its SpaceShipOne.) Today, Angel's Web site, which remains untouched since 2001, stands as an artifact of the optimistic era. Now-defunct Skystation International, which former Secretary of State Alexander Haig headed, fared no better in its plan to use helium-filled dirigibles. Sanswire Networks (www.sanswire.com) has flown autonomous craft like the one in this photo but has yet to serve customers.

Rapid buildup of terrestrial wireless and wire-line networks closed a narrow launch window for these companies, says Craig Mathias, principal with Farpoint Group (www.farpointgroup.com). "But it's still an intriguing idea," he says. "I'm sure somebody's going to try it." For example, a stratospheric platform might well suit use in delivering digital-TV channels or, given its immunity to terrestrial disasters, delivering emergency-communications services, he says.—by Matthew Miller

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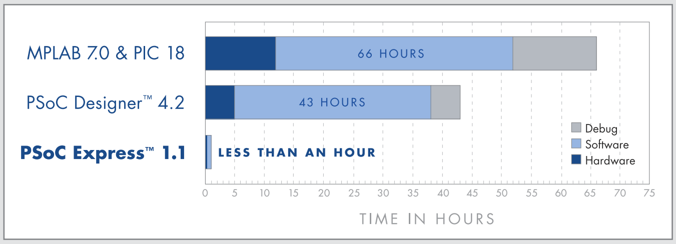

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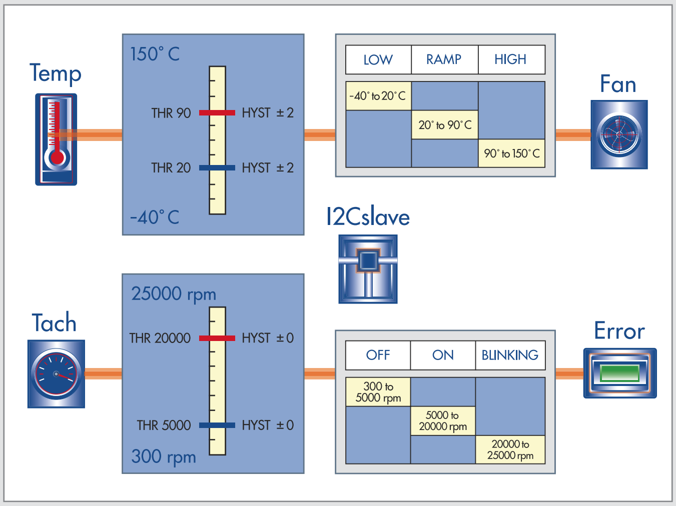

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